New Products and Updated Product Data Sheets

IGBT UFS SERIES SUPPLEMENT

1997

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- **Internet: http://www.semi.harris.com**
- **AnswerFAX: 1-407-724-7800**
- **Technical Assistance: E-mail centapp@harris.com**

First Name ______________ (PLEASE PRINT) Last Name ______________ (PLEASE PRINT) MI ______

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City ______________ State ______ Zip ______ Country ______

Phone ______________ Fax ______________ E-Mail ______

❑ **Add my name to your mailing list.**

1. Do you have access to CD-ROM capabilities?
   ❑ At Work ❑ At Home ❑ No
2. Do you have access to the Internet?
   ❑ At Work ❑ At Home ❑ No
3. What is your preferred source of product data sheets? (select one)
   ❑ Data Books ❑ CD-ROM ❑ Internet
   ❑ AnswerFAX ❑ Stand-Alone Data Sheets
4. Would you prefer to have a CD-ROM Data Book, a printed Data Book, or both?
   ❑ CD-ROM Book ❑ Printed Book ❑ Both
5. Which best describes your current design stage (select one):
   ❑ Info Collection ❑ Initial Production
   ❑ Prototyping ❑ Breadboarding
   ❑ Design Concept ❑ Full Production
6. When will your design be finalized?
   Month ______ Year ______
7. Expected Annual Volume at full production (select one):
   ❑ 1 to 999 ❑ 5K to 100K
   ❑ 1K to 4999 ❑ > 100K
8. This location has as its primary function (select one)
   ❑ Manufacturing ❑ Design
   ❑ Both

Which category best describes your primary end market? (Select One) ☐

1100 Video/Imaging
1101 - Desktop Multimedia
1102 - Prof/Broadcast Video
1103 - Medical Imaging
1104 - Cable TV
1105 - Video Conferencing
1199 - Other Video/Imaging

1200 Wireless Communication
1201 - Base Stations
1202 - Wireless LAN/PCS/PB
1203 - Handset/Terminals
1204 - Satellite Communication
1205 - Wireless Local Loop
1299 - Other Wireless Comm.

1300 Government/Military
1301 - Space
1302 - Guidance/Control
1303 - Radar
1304 - Communications
1305 - Avionics
1399 - General Gov't/Military

1400 Telecom
1401 - PBX or CO Line Cards
1402 - Fiber-in-the-Loop
1403 - Wireless Local Loop
1404 - Fiber Optics
1405 - ADSL/HDSL
1406 - Other High Speed Datacomm
1499 - Other Telecom

1500 Computers/Peripherals
1501 - Laptops/Palmtops
1502 - Desktop PCs
1503 - Workstation/File Server
1504 - Disk/Tape Drives
1505 - Printers/Plotter/Scanner
1506 - Datacomm
1599 - General Computer/EDP

1600 Transportation/Consumer
1601 - Power Train
1602 - Vehicle Control
1603 - Safety & Convenience
1604 - Driver Information
1605 - Entertainment
1606 - Electric Vehicles
1607 - Consumer
1699 - Other Transportation

1700 Power Supply/Power Mgmt
1701 - UPS (Uninterruptible Power Supplies)
1702 - AC-DC Power Supplies
1703 - DC-DC Power Supplies
1704 - Transmission Lines
1705 - Utility Substations
1706 - Panel Boxes
1707 - General Protection
1799 - Other Power Supplies/Mgmt

1800 Motor Control
1801 - AC Motors
1802 - 3 Phase Motors
1803 - Brushless
1804 - DC Motors
1805 - Stepper Motors
1899 - Other Motor Control

1900 Industrial Controls & Instrumentation
1901 - Manufacturing System
1902 - High Speed Instrumentation
1903 - Handheld Instruments
1904 - Medical Electronics
1905 - HVAC
1906 - Automatic Test Equipment (ATE)
1999 - General Industrial & Instrumentation

2000 Other Electronics, Not Listed Above

Which best describes your job function? (select one):
❑ Consultant
❑ Corporate/Operating Management
❑ Documentation
❑ Education
❑ Engineering
❑ Manufacturing
❑ Marketing
❑ Purchasing
❑ Quality Assurance
❑ Sales
❑ Systems

What is your primary product interest? (select one):
❑ Analog
❑ Protection Devices
❑ Power Control
❑ Converter
❑ Digital
❑ DSP
❑ Telecom
❑ Rad Hard
❑ Power Discrete
❑ Multimedia
❑ Wireless

Which best describes your job responsibility (select one):
❑ President/Owner
❑ Vice-President/Director
❑ Manager/Section Head
❑ Engineer
❑ Assistant
❑ Independent Contractor

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HARRIS IGBT DATA BOOKS

The UFS series IGBT (Insulated Gate Bipolar Transistor) Data Book Supplement represents a new generation of IGBT products for commercial applications from Harris Semiconductor Discrete Power Product Line. This data book supplement describes Harris Semiconductor's line of UFS (Ultra Fast Switching) IGBTs. The MCT/IGBT/Diodes Databook (DB309) represents the full line of these products made by Harris Semiconductor Discrete Power products for commercial applications. For a complete listing of Harris Semiconductor products, please refer to the Product Selection Guide (PSG-201, ordering information below).

For complete, current and detailed technical specifications on any Harris device please contact the nearest Harris sales, representative or distributor office (see Section 10). Literature requests may also be directed to the address listed below.

UFS SERIES IGBT PRODUCTS

Harris Semiconductor is a leader in IGBT technology. Our UFS series delivers solid advantages over other system solutions. The UFS Series IGBTs offer some of the lowest saturation voltages and turn losses; combined with some of the highest current densities in the IGBT market. The UFS series IGBTs will reduce your parts count, and lower your total system cost. You can also operate at higher frequencies, reduce your conduction losses, and improve your circuits fault tolerance. Applications for the UFS Series IGBT include Switched Mode Power Supplies (SMPS), resonant mode power supplies, motor controls, DC servos, robotic drives, Uninterruptible Power Supplies (UPS), battery chargers, and welders.

Harris's commitment to total quality management has no limits. Every Harris Semiconductor Manufacturing facility world wide, has been audited and certified as ISO9002 compliant. In fact, in many areas, Harris' own quality criteria are even more rigorous then those of International Standards Organization (ISO), resulting in the highest quality products, and excellent on time delivery. With our dedicated people, and world class products, Harris Semiconductor is prepared to excel in tomorrow's market place as well as today's.

It is our intention to provide you with the most up-to-date information on our products. For complete, current and detailed technical specifications on any Harris device, please contact the nearest Harris sales representative or distributor office, listed at the end of the databook; or direct literature request to:

Harris Semiconductor Literature Department
P.O. Box 883, MS 53-204
Melbourne, FL 32902
Phone: 1-800-442-7747
FAX: 407-724-7240
AnswerFAX: 407-724-7800

This catalog is an invaluable reference for engineers and technicians in the communications field. Please contact your local sales office listed in Section 10 for further assistance.

For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG201; ordering information above).

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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IGBT UFS SERIES SUPPLEMENT

FOR COMMERCIAL APPLICATIONS

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IGBT UFS SERIES SUPPLEMENT 1

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C-SPEED UFS SERIES IGBTs

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IGBT UFS SERIES SUPPLEMENT 2

UFS SERIES IGBT LINE CARD

PAGE

Line Card

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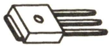
HARRIS SEMICONDUCTOR

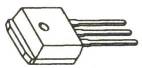
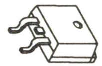
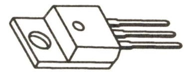
600V UFS Series IGBTs

$V_{CE(SAT)}$
Maximum at $T_J = +25^oC$
$I_{CE} = I_{C110}$, and $V_{GE} = 15V$

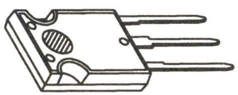
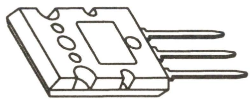
E_{OFF}
Typical at $T_J = +150^oC$
$I_{CE} = I_{C110}$, and $V_{CE(PK)} = 480V$




I_C AT 110°C	TO-251AA (D-PAK)			TO-252AA (D-PAK)		
	600V 275ns UFS	**600V 200ns UFS**	**600V RUGGED UFS**	**600V 275ns UFS**	**600V 200ns UFS**	**600V RUGGED UFS**
3A	HGTD3N60C3 2.0V 245µJ	*HGTD3N60B3* 2.0V 200µJ	*HGTD3N60C3R* 2.3V TBD µJ	HGTD3N60C3S 2.0V 245µJ	*HGTD3N60B3S* 2.0V 200µJ	*HGTD3N60C3RS* 2.3V TBD µJ
7A	HGTD7N60C3 2.0V 600µJ	*HGTD7N60B3* 2.0V 350µJ	*HGTD7N60C3R* 2.3V TBD µJ	HGTD7N60C3S 2.0V 600µJ	*HGTD7N60B3S* 2.0V 350µJ	*HGTD7N60C3RS* 2.3V TBD µJ

I_C AT 110°C	TO-262AA (D^2-PAK)			TO-263AB (D^2-PAK)			TO-220AB		
	600V 275ns UFS	**600V 200ns UFS**	**600V RUGGED UFS**	**600V 275ns UFS**	**600V 200ns UFS**	**600V RUGGED UFS**	**600V 275ns UFS**	**600V 200ns UFS**	**600V RUGGED UFS**
3A	HGT1S3N60C3D 2.0V 245µJ	*HGT1S3N60B3D* 2.0V 200µJ	*HGT1S3N60C3DR* 2.3V TBD µJ	HGT1S3N60C3DS 2.0V 245µJ	*HGT1S3N60B3DS* 2.0V 200µJ	*HGT1S3N60C3DRS* 2.3V TBD µJ	HGTP3N60C3D 2.0V 245µJ	*HGTP3N60B3D* 2.0V 200µJ	*HGTP3N60C3DR* 2.3V TBD µJ
7A	HGT1S7N60C3D 2.0V 600µJ	*HGT1S7N60B3D* 2.0V 350µJ	*HGT1S7N60C3DR* 2.3V TBD µJ	HGT1S7N60C3DS 2.0V 600µJ	*HGT1S7N60B3DS* 2.0V 350µJ	*HGT1S7N60C3DRS* 2.3V TBD µJ	HGTP7N60C3 HGTP7N60C3D 2.0V 600µJ	*HGTP7N60B3D* 2.0V 350µJ	*HGTP7N60C3DR* 2.3V TBD µJ
12A	HGT1S12N60C3 HGT1S12N60C3D 2.0V 900µJ	*HGT1S12N60B3* *HGT1S12N60B3D* 2.0V 800µJ	*HGT1S12N60C3R* *HGT1S12N60C3DR* 2.3V TBD µJ	HGT1S12N60C3S HGT1S12N60C3DS 2.0V 900µJ	*HGT1S12N60B3S* *HGT1S12N60B3DS* 2.0V 800µJ	*HGT1S12N60C3RS* *HGT1S12N60C3DRS* 2.3V TBD µJ	HGTP12N60C3 HGTP12N60C3D 2.0V 900µJ	*HGTP12N60B3* *HGTP12N60B3D* 2.0V 800µJ	*HGTP12N60C3R* *HGTP12N60C3DRS* 2.3V TBD µJ
20A	*HGT1S20N60C3* 1.8V 1500µJ	HGT1S20N60B3 2.0V 1050µJ	HGT1S20N60C3R 2.3V 3000µJ	*HGT1S20N60C3S* 1.8V 1500µJ	HGT1S20N60B3S 2.0V 1050µJ	HGT1S20N60C3RS 2.3V 3000µJ	*HGTP20N60C3* 1.8V 1500µJ	HGTP20N60B3 2.0V 1050µJ	HGTP20N60C3R 2.3V 3000µJ

I_C AT 110°C	TO-247			TO-264		
	600V 275ns UFS	**600V 200ns UFS**	**600V RUGGED UFS**	**600V 275ns UFS**	**600V 200ns UFS**	**600V RUGGED UFS**
12A	HGTG12N60C3D 2.0V 900µJ	*HGTG12N60B3D* 2.0V 800µJ	*HGTG12N60C3DR* 2.3V TBD µJ			
20A	*HGTG20N60C3* *HGTG20N60C3D* 1.8V 1500µJ	HGTG20N60B3 HGTG20N60B3D 2.0V 1050µJ	HGTG20N60C3R HGTG20N60C3DR 2.3V 3000µJ			
30A	HGTG30N60C3 HGTG30N60C3D 1.8V 2500µJ	*HGTG30N60B3* *HGTG30N60B3D* 2.2V 1700µJ	*HGTG27N60C3R* *HGTG27N60C3DR* 2.3V 2000µJ			
40A	*HGTG40N60C3* 1.6V 3300µJ	HGTG40N60B3 2.0V 2500µJ	*HGTG40N60C3R* 2.3V TBD µJ	*HGT1Y40N60C3D* 1.6V 3300µJ	*HGT1Y40N60B3D* 2.0V 2500µJ	*HGT1Y40N60C3DR* 2.3V TBD µJ

PART NOMENCLATURE

HGT - G - 12 - N - 60 - C - 3 - D

HARRIS IGBT

PACKAGE
- D: 3 Lead TO-251/TO-252
- 1S: 3 Lead TO-262/TO-263
- P: 3 Lead TO-220
- G: 3 Lead TO-247
- 1Y: 3 Lead TO-264

CONTINUOUS CURRENT
Rating at $T_C = +110^oC$

POLARITY
N-Channel or P-Channel

VOLTAGE BREAKDOWN/10
i.e. (60, 120)

MAX FALL TIME AT $T_J = +150^oC$
- A: 100ns
- B: 200ns
- C: 500ns
- D: 750ns
- E: ≤1µs
- F: ≤2µs
- G: ≤5µs

- 1: First Generation
- 2: Second Generation
- 3: Third Generation

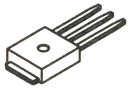
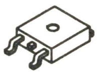
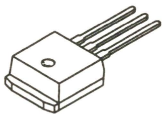
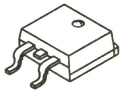
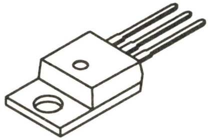
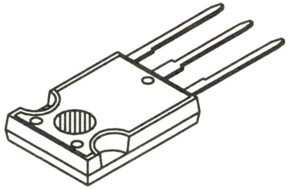
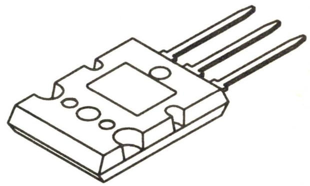
OPTIONS
- L: Logic Level Gate
- D: Integral Reverse Diode
- S: Surface Mount
- C: Current Sense
- V: Voltage Clamping
- R: Rugged IGBT

LC96585.1

HARRIS SEMICONDUCTOR

1200V UFS Series IGBTs

$V_{CE(SAT)}$	E_{OFF}
Maximum at $T_J = +25^oC$ $I_{CE} = I_{C110}$, and $V_{GE} = 15V$	Typical at $T_J = +150^oC$ $I_{CE} = I_{C110}$, and $V_{CE(PK)} = 960V$

	 TO-251AA (D-PAK)	 TO-252AA (D-PAK)	 TO-262AA (D^2-PAK)	 TO-263AB (D^2-PAK)	 TO-220AB	 TO-247	 *TO-264*
I_C AT 110^oC	1200V 400ns UFS	1200V 400ns UFS	1200V 400ns UFS	1200V 400ns UFS	1200V 400ns UFS	1200V 400ns UFS	1200V 400ns UFS
3A	*HGTD3N120C3* 3.0V TBD µJ	*HGTD3N120C3S* 3.0V TBD µJ	*HGT1S3N120C3D* 3.0V TBD µJ	*HGT1S3N120C3DS* 3.0V TBD µJ	*HGTP3N120C3D* 3.0V TBD µJ		
5A	*HGTD5N120C3* 3.0V TBD µJ	*HGTD5N120C3S* 3.0V TBD µJ	*HGT1S5N120C3D* 3.0V TBD µJ	*HGT1S5N120C3DS* 3.0V TBD µJ	*HGTP5N120C3D* 3.0V TBD µJ		
10A			*HGT1S10N120C3* *HGT1S10N120C3D* 3.0V 3200µJ	*HGT1S10N120C3S* *HGT1S10N120C3SD* 3.0V 3200µJ	*HGTP10N120C3* *HGTP10N120C3D* 3.0V 3200µJ	*HGTG10N120C3D* 3.0V 3200µJ	
15A			*HGT1S15N120C3* 3.0V 4700µJ	*HGT1S15N120C3S* 3.0V 4700µJ	HGTP15N120C3 3.0V 4700µJ	*HGTG15N120C3, HGTG15N120C3D* 3.0V 4700µJ	
20A						*HGTG20N120C3, HGTG20N120C3D* 3.0V 6300µJ	
30A						*HGTG30N120C3* 3.0V 9400µJ	*HGT1Y30N120C3D* 3.0V 9400µJ

1200V 300ns UFS and Rugged UFS products to be offered in the future.

ITALICS = Future Product Offerings

LC96585.1

IGBT UFS SERIES SUPPLEMENT 3

C-SPEED UFS SERIES IGBTs

		PAGE
C-Speed UFS Series IGBT Data Sheets		
HGTD3N60C3, HGTD3N60C3S	6A, 600V, UFS Series N-Channel IGBTs	3-3
HGTP3N60C3D, HGT1S3N60C3D, HGT1S3N60C3DS	6A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diodes	3-9
HGTD7N60C3, HGTD7N60C3S, HGTP7N60C3	14A, 600V, UFS Series N-Channel IGBTs	3-16
HGTP7N60C3D, HGT1S7N60C3D, HGT1S7N60C3DS	14A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diodes	3-22
HGTP12N60C3, HGT1S12N60C3, HGT1S12N60C3S	24A, 600V, UFS Series N-Channel IGBTs	3-29
HGTG12N60C3D	24A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode	3-35
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HGTG30N60C3	63A, 600V, UFS Series N-Channel IGBT	3-49
HGTG30N60C3D	63A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode	3-55

HARRIS SEMICONDUCTOR

HGTD3N60C3, HGTD3N60C3S

January 1997

6A, 600V, UFS Series N-Channel IGBTs

Features

- **6A, 600V at $T_C = 25^oC$**
- **600V Switching SOA Capability**
- **Typical Fall Time . . . . 130ns at $T_J = 150^oC$**
- **Short Circuit Rating**
- **Low Conduction Loss**

Description

The HGTD3N60C3 and HGTD3N60C3S are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors

PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTD3N60C3	TO-251AA	G3N60C
HGTD3N60C3S	TO-252AA	G3N60C

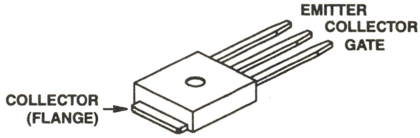
NOTE: When ordering, use the entire part number.

Add the suffix 9A to obtain the TO-252AA variant in Tape and Reel, i.e. HGTD3N60C3S9A.

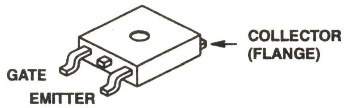
Formerly developmental type TA49113.

Packaging

JEDEC TO-251AA

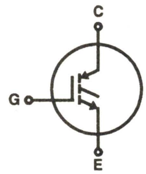


JEDEC TO-252AA



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



3

C-SPEED UFS SERIES

Absolute Maximum Ratings $T_A = 25^oC$

		HGTD3N60C3 HGTD3N60C3S	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	6	A
At $T_C = 110^oC$	I_{C110}	3	A
Collector Current Pulsed (Note 1)	I_{CM}	24	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Figure 14	SSOA	18A at 480V	
Power Dissipation Total at $T_C = 25^oC$	P_D	33	W
Power Dissipation Derating $T_C > 25^oC$		0.27	W/°C
Reverse Voltage Avalanche Energy	E_{ARV}	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$, Figure 6	t_{SC}	8	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = 125^oC$, $R_{GE} = 82\Omega$.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 3mA$, $V_{GE} = 0V$		16	30	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	2.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.65	2.0	V
			$T_C = 150^oC$	-	1.85	2.2	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.0	5.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm25V$		-	-	±250	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 82\Omega$, $V_{GE} = 15V$, $L = 1mH$	$V_{CE(PK)} = 480V$	18	-	-	A
			$V_{CE(PK)} = 600V$	2	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8.3	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	10.8	13.5	nC
			$V_{GE} = 20V$	-	13.8	17.3	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 82\Omega$, $L = 1mH$		-	5	-	ns
Current Rise Time	t_{RI}			-	10	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	325	400	ns
Current Fall Time	t_{FI}			-	130	275	ns
Turn-On Energy	E_{ON}			-	85	-	µJ
Turn-Off Energy (Note 3)	E_{OFF}			-	245	-	µJ
Thermal Resistance	$R_{\theta JC}$			-	-	3.75	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTD3N60C3 and HGTD3N60C3S were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951

Typical Performance Curves

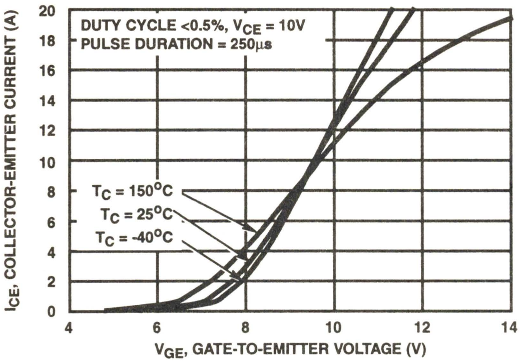


FIGURE 1. TRANSFER CHARACTERISTICS

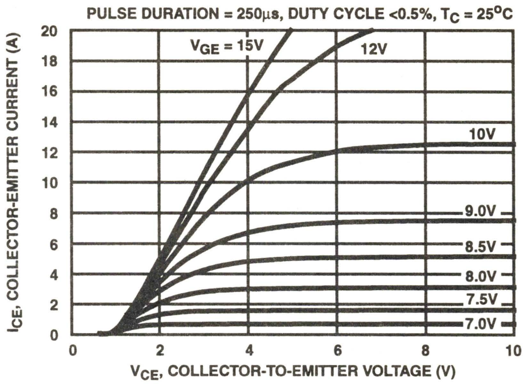


FIGURE 2. SATURATION CHARACTERISTICS

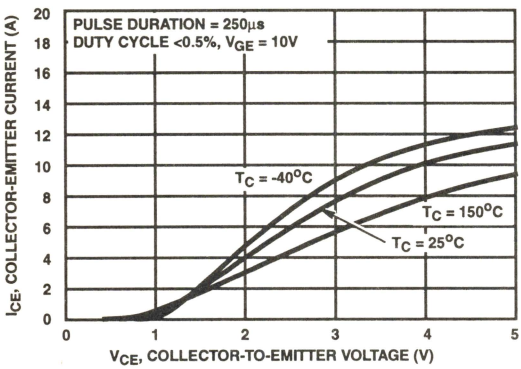


FIGURE 3. COLLECTOR-EMITTER ON-STATE VOLTAGE

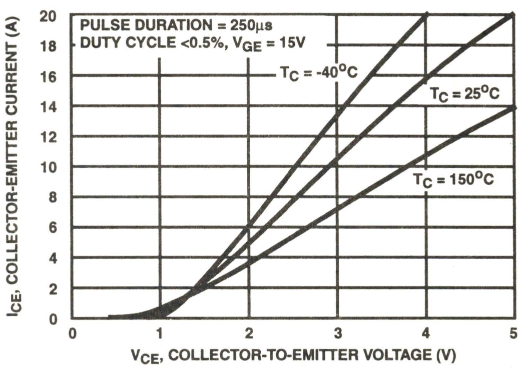


FIGURE 4. COLLECTOR-EMITTER ON-STATE VOLTAGE

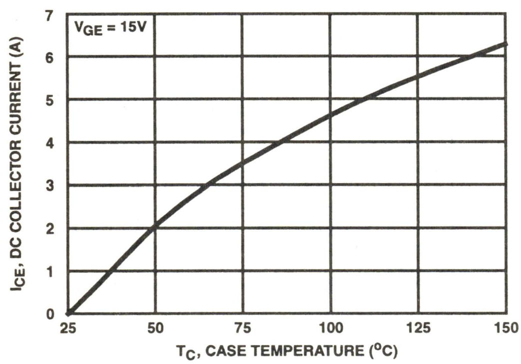


FIGURE 5. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

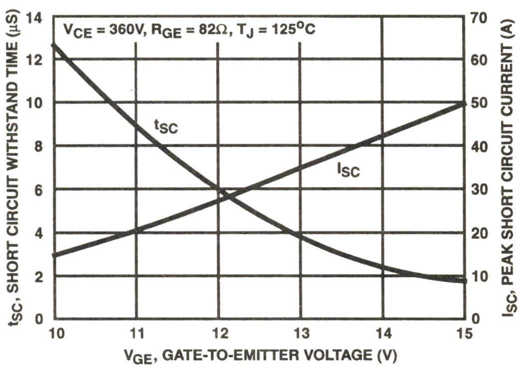


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

3

C-SPEED UFS SERIES

Typical Performance Curves (Continued)

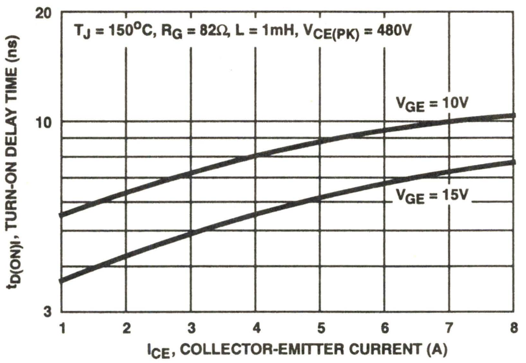


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

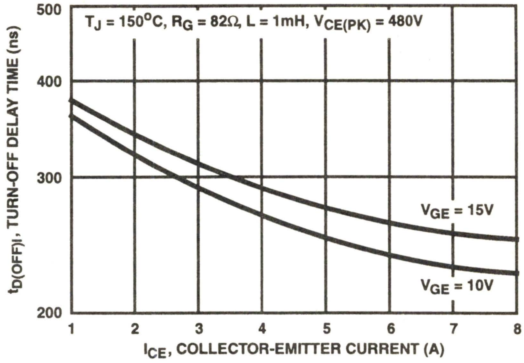


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

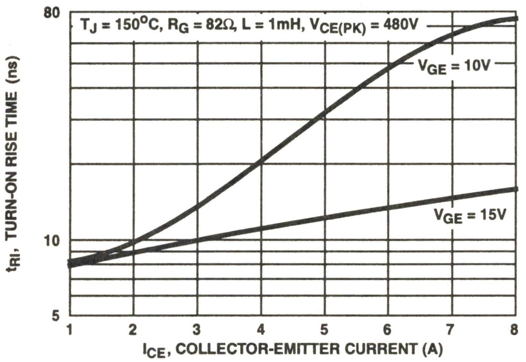


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

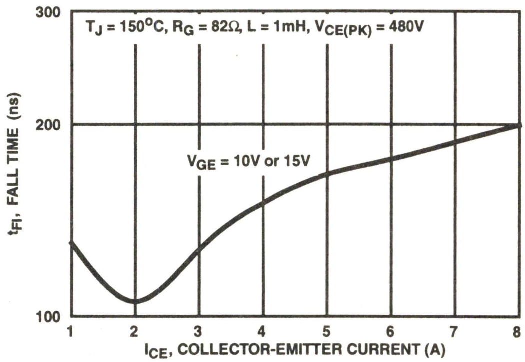


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

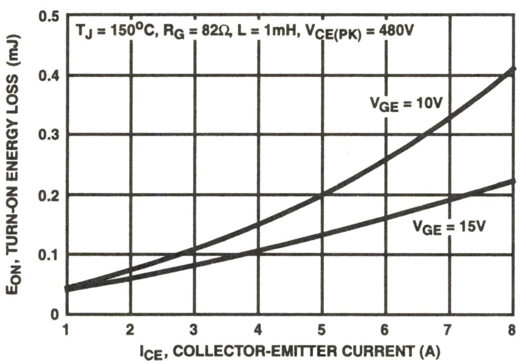


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

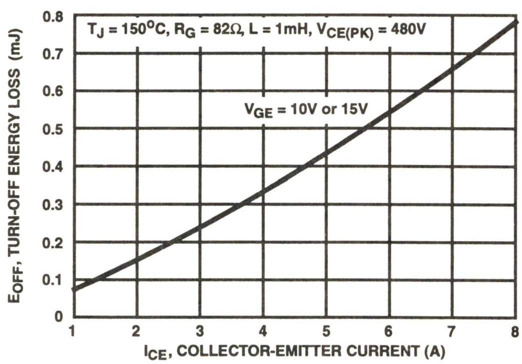


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

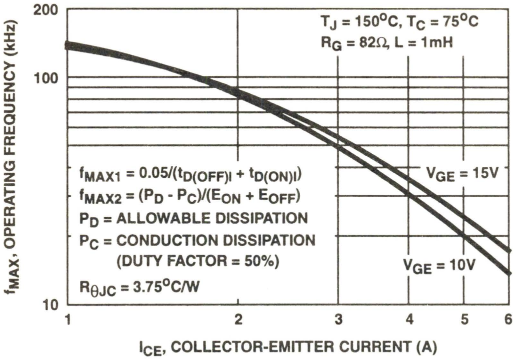


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

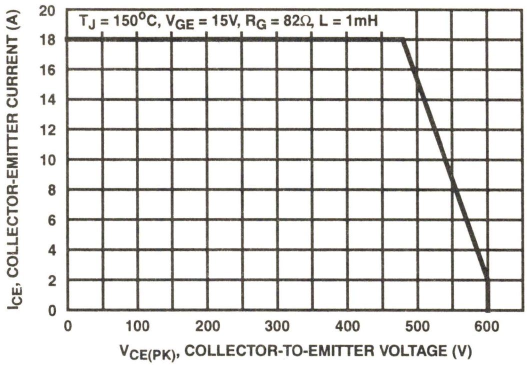


FIGURE 14. MINIMUM SWITCHING SAFE OPERATING AREA

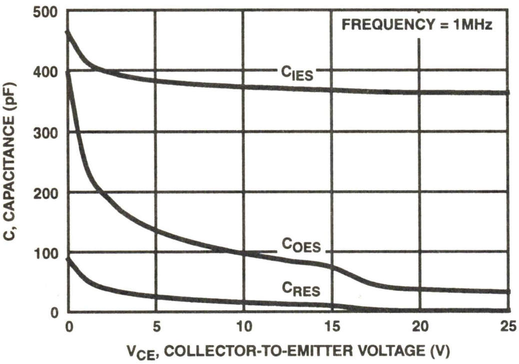


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

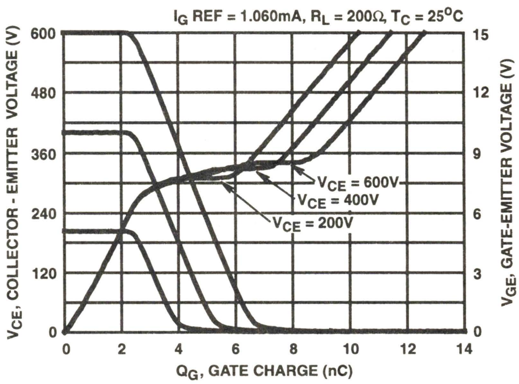


FIGURE 16. GATE CHARGE WAVEFORMS

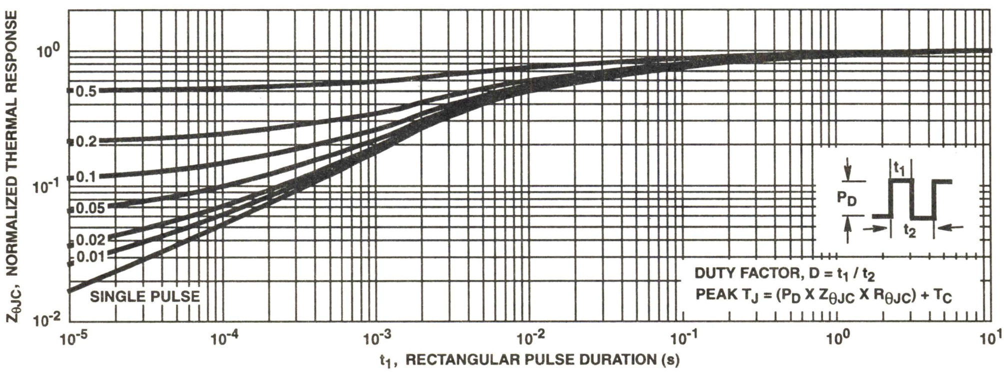


FIGURE 17. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Test Circuit and Waveform

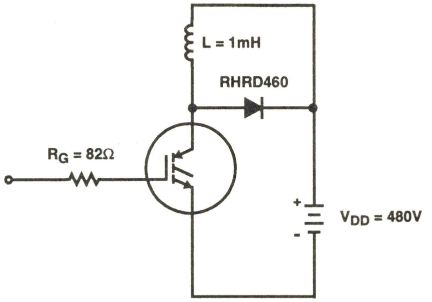


FIGURE 18. INDUCTIVE SWITCHING TEST CIRCUIT

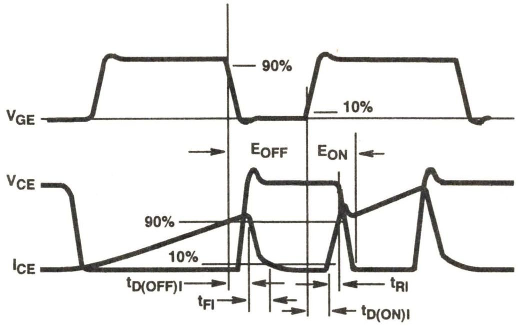


FIGURE 19. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBT's are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

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Operating Frequency Information

Operating Frequency Information for a Typical Device

Figure 13 is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 19.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$. E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 19. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

HARRIS SEMICONDUCTOR

HGTP3N60C3D, HGT1S3N60C3D, HGT1S3N60C3DS

6A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diodes

January 1997

Features

- 6A, 600V at $T_C = 25^oC$
- 600V Switching SOA Capability
- Typical Fall Time .... 130ns at $T_J = 150^oC$
- Short Circuit Rating
- Low Conduction Loss
- Hyperfast Anti-Parallel Diode

Description

The HGTP3N60C3D, HGT1S3N60C3D, and HGT1S3N60C3DS are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25^oC and 150^oC. The IGBT used is the development type TA49113. The diode used in anti-parallel with the IGBT is the development type TA49055.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential.

PACKAGING AVAILABILITY

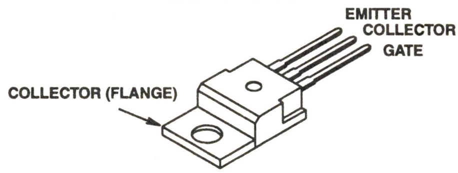
PART NUMBER	PACKAGE	BRAND
HGTP3N60C3D	TO-220AB	G3N60C3D
HGT1S3N60C3D	TO-262AA	G3N60C3D
HGT1S3N60C3DS	TO-263AB	G3N60C3D

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, i.e. HGT1S3N60C3DS9A.

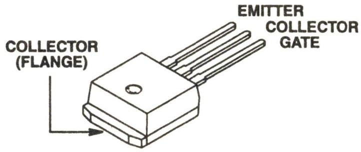
Formerly Developmental Type TA49119.

Packaging

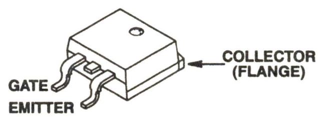
JEDEC TO-220AB



JEDEC TO-262AA

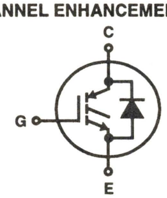


JEDEC TO-263AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTP3N60C3D, HGT1S3N60C3D HGT1S3N60C3DS	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	6	A
At $T_C = 110^oC$	I_{C110}	3	A
Collector Current Pulsed (Note 1)	I_{CM}	24	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Fig. 14	SSOA	18A at 480V	
Power Dissipation Total at $T_C = 25^oC$	P_D	33	W
Power Dissipation Derating $T_C > 25^oC$		0.27	W/^oC
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	^oC
Maximum Lead Temperature for Soldering	T_L	260	^oC
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$, Fig 6	t_{SC}	8	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = 125^oC$, $R_{GE} = 82\Omega$.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	2.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.65	2.0	V
			$T_C = 150^oC$	-	1.85	2.2	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.0	5.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 25V$		-	-	±250	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 82\Omega$, $V_{GE} = 15V$, $L = 1mH$	$V_{CE(PK)} = 480V$	18	-	-	A
			$V_{CE(PK)} = 600V$	2	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8.3	-	V
On-State Gate Charge	$Q_{G(ON)}$	IC = IC110, VCE = 0.5 BVCES	$V_{GE} = 15V$	-	10.8	13.5	nC
			$V_{GE} = 20V$	-	13.8	17.3	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 82\Omega$, $L = 1mH$		-	5	-	ns
Current Rise Time	t_{RI}			-	10	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	325	400	ns
Current Fall Time	t_{FI}			-	130	275	ns
Turn-On Energy	E_{ON}			-	85	-	µJ
Turn-Off Energy (Note 3)	E_{OFF}			-	245	-	µJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 3A$		-	2.0	2.5	V
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 3A$, $dI_{EC}/dt = 200A/\mu s$		-	22	28	ns
		$I_{EC} = 1A$, $dI_{EC}/dt = 200A/\mu s$		-	17	22	ns
Thermal Resistance	$R_{\theta JC}$	IGBT		-	-	3.75	$^oC/W$
		Diode		-	-	3.0	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTP3N60C3D, HGT1S3N60C3D, and HGT1S3N60C3DS were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951

Typical Performance Curves

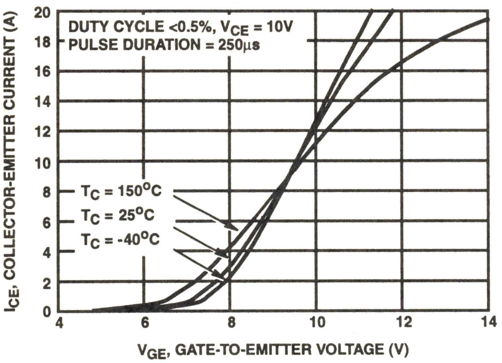


FIGURE 1. TRANSFER CHARACTERISTICS

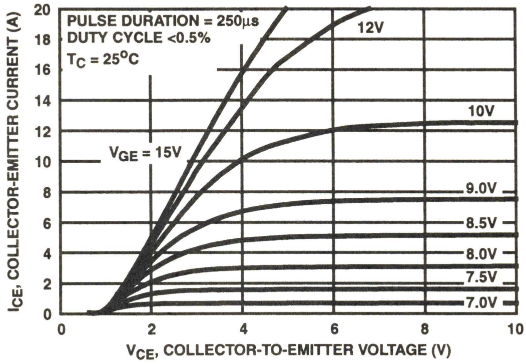


FIGURE 2. SATURATION CHARACTERISTICS

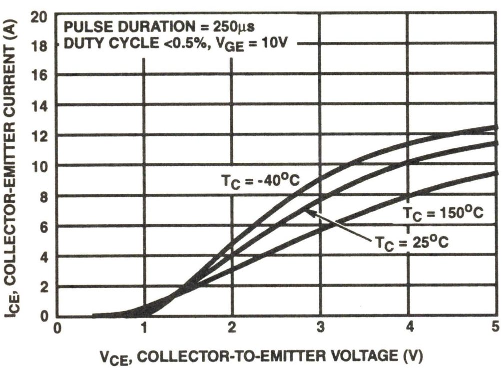


FIGURE 3. COLLECTOR-EMITTER ON - STATE VOLTAGE

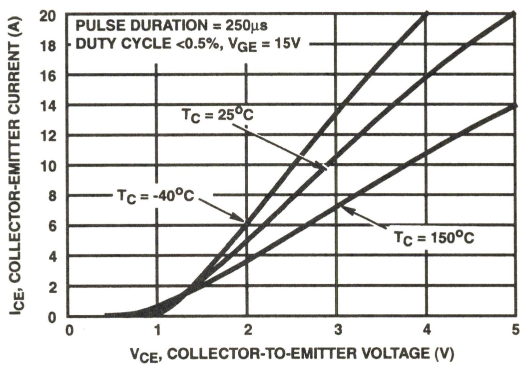


FIGURE 4. COLLECTOR-EMITTER ON - STATE VOLTAGE

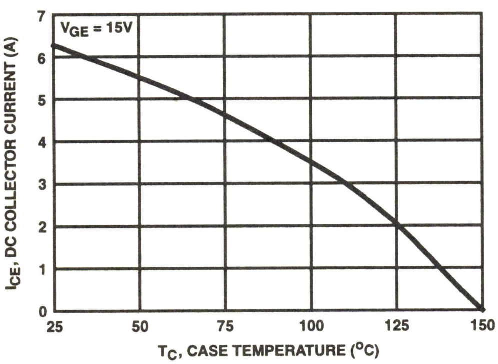


FIGURE 5. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

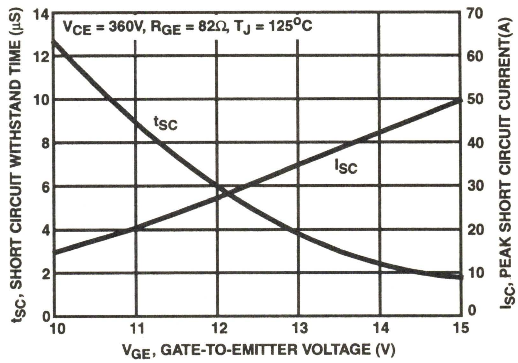


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

3

C-SPEED UFS SERIES

Typical Performance Curves (Continued)

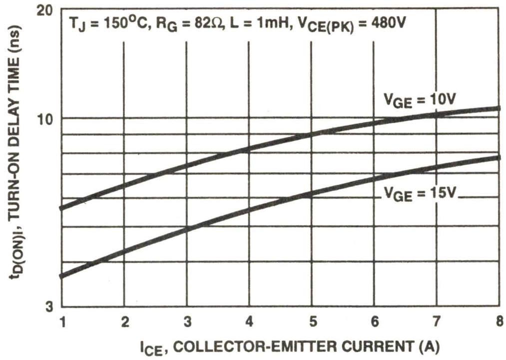


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

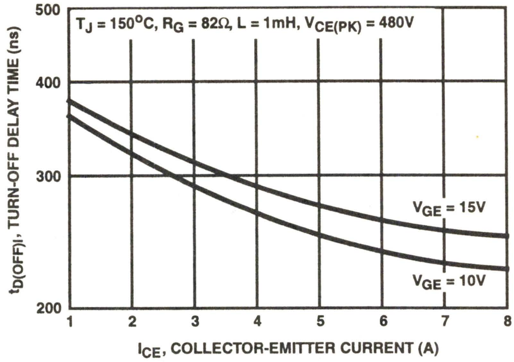


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

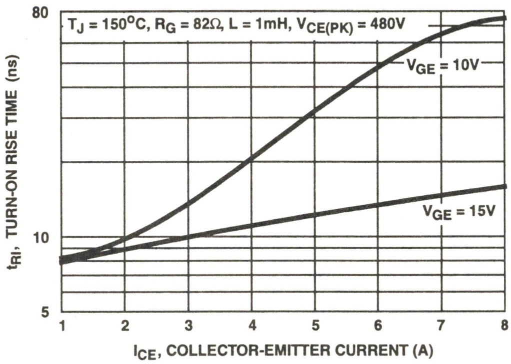


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

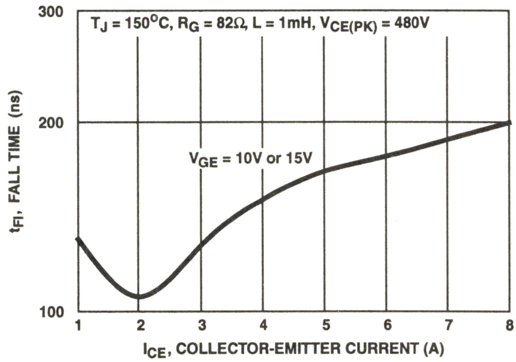


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

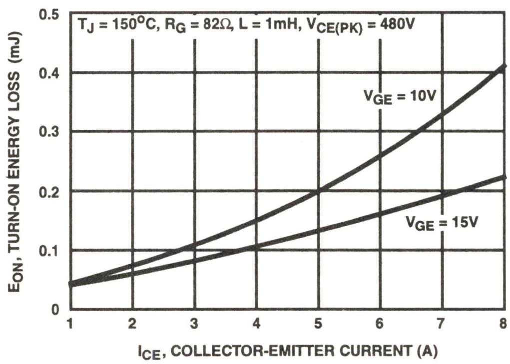


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

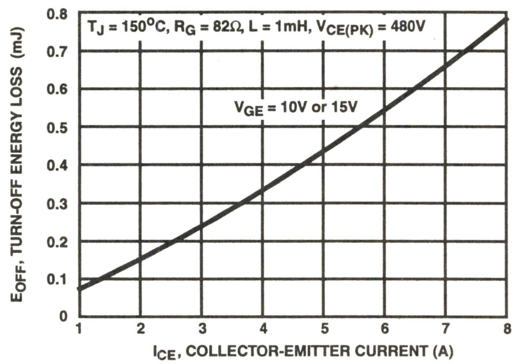


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

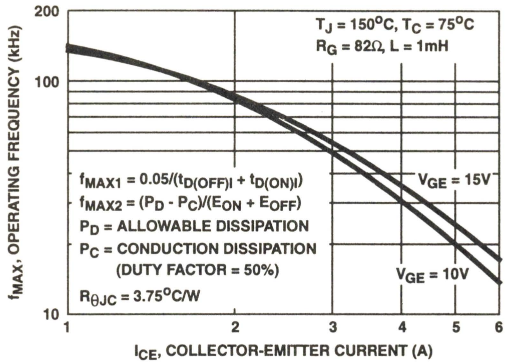


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

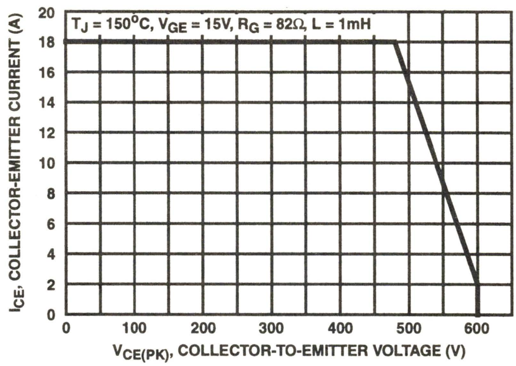


FIGURE 14. MINIMUM SWITCHING SAFE OPERATING AREA

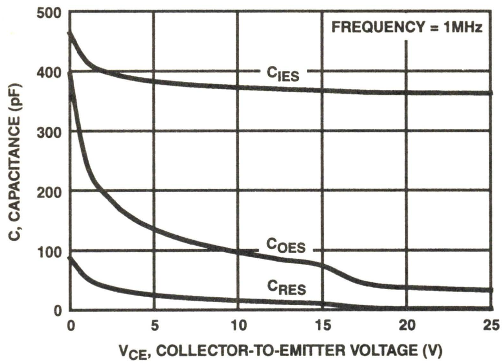


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

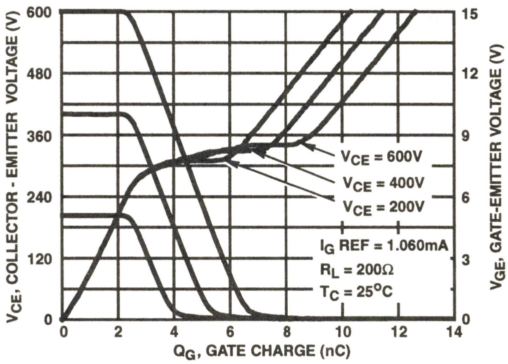


FIGURE 16. GATE CHARGE WAVEFORMS

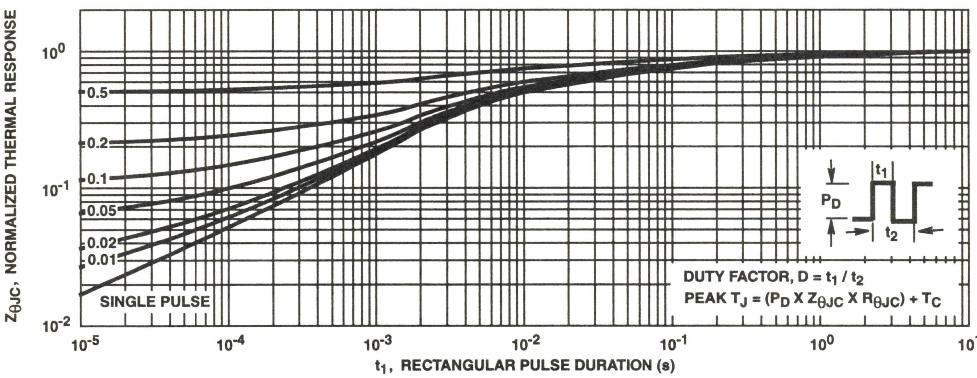


FIGURE 17. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Typical Performance Curves (Continued)

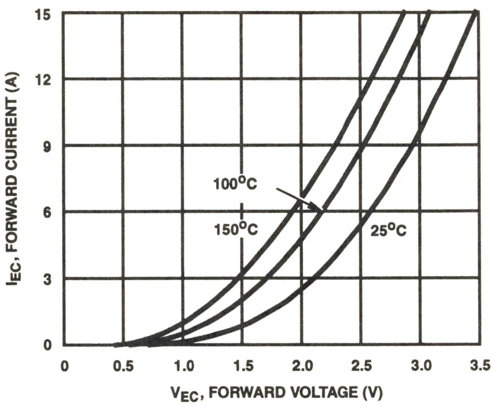


FIGURE 18. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

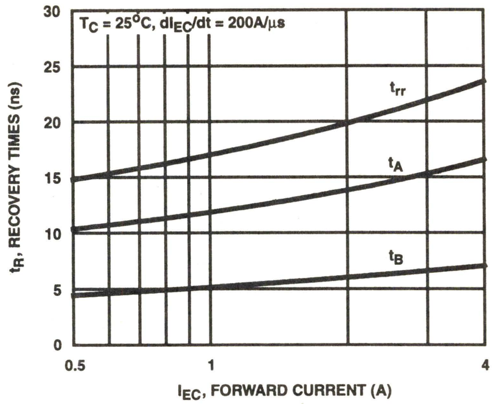


FIGURE 19. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveform

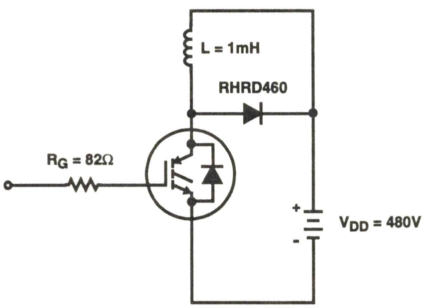


FIGURE 20. INDUCTIVE SWITCHING TEST CIRCUIT

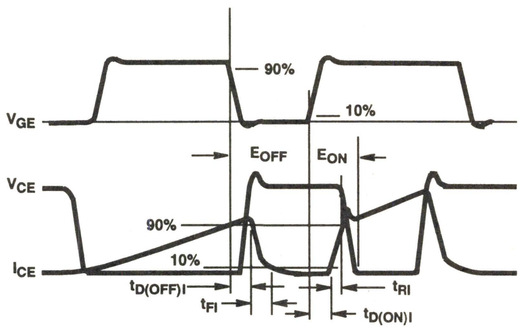


FIGURE 21. SWITCHING TEST WAVEFORMS

Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 21.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 21. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as ECCOSORBD™ LD26 or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

ECCOSORBD™ is a Trademark of Emerson and Cumming, Inc.

HARRIS SEMICONDUCTOR

HGTD7N60C3, HGTD7N60C3S, HGTP7N60C3

January 1997

14A, 600V, UFS Series N-Channel IGBTs

Features

- 14A, 600V at $T_C = 25^oC$
- 600V Switching SOA Capability
- Typical Fall Time . . . . 140ns at $T_J = 150^oC$
- Short Circuit Rating
- Low Conduction Loss

Description

The HGTD7N60C3, HGTD7N60C3S and HGTP7N60C3 are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTD7N60C3	TO-251AA	G7N60C
HGTD7N60C3S	TO-252AA	G7N60C
HGTP7N60C3	TO-220AB	G7N60C3

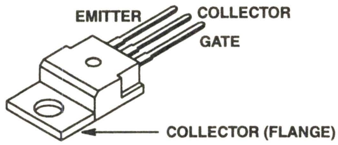
NOTE: When ordering, use the entire part number.

Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e. HGTD7N60C3S9A.

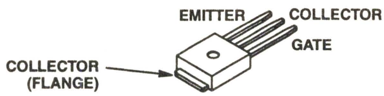
Formerly Developmental Type TA49115.

Packaging

JEDEC TO-220AB



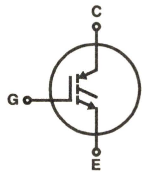
JEDEC TO-251AA



JEDEC TO-252AA

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTD7N60C3, HGTD7N60C3S HGTP7N60C3	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	14	A
At $T_C = 110^oC$	I_{C110}	7	A
Collector Current Pulsed (Note 1)	I_{CM}	56	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Figure 14	SSOA	40A at 480V	
Power Dissipation Total at $T_C = 25^oC$	P_D	60	W
Power Dissipation Derating $T_C > 25^oC$		0.48	W/°C
Reverse Voltage Avalanche Energy	E_{ARV}	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	1	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	8	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = 125^oC$, $R_{GE} = 50\Omega$.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 3mA$, $V_{GE} = 0V$		16	30	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	2.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.6	2.0	V
			$T_C = 150^oC$	-	1.9	2.4	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.0	5.0	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 25V$		-	-	±250	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 50\Omega$, $V_{GE} = 15V$, $L = 1mH$	$V_{CE(PK)} = 480V$	40	-	-	A
			$V_{CE(PK)} = 600V$	6	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	23	30	nC
			$V_{GE} = 20V$	-	30	38	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 50\Omega$, $L = 1.0mH$		-	8.5	-	ns
Current Rise Time	t_{RI}			-	11.5	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	350	400	ns
Current Fall Time	t_{FI}			-	140	275	ns
Turn-On Energy	E_{ON}			-	165	-	µJ
Turn-Off Energy (Note 3)	E_{OFF}			-	600	-	µJ
Thermal Resistance	$R_{\theta JC}$			-	-	2.1	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTD7N60C3, HGTD7N60C3S and HGTP7N60C3 were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951

Typical Performance Curves

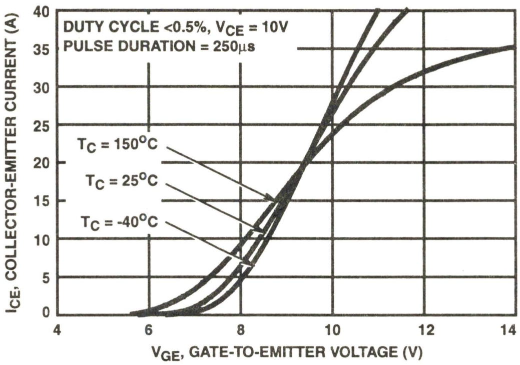


FIGURE 1. TRANSFER CHARACTERISTICS

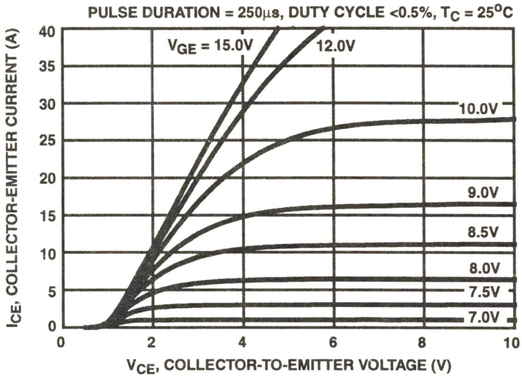


FIGURE 2. SATURATION CHARACTERISTICS

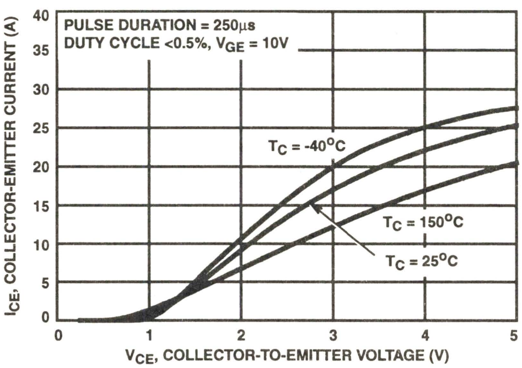


FIGURE 3. COLLECTOR-EMITTER ON - STATE VOLTAGE

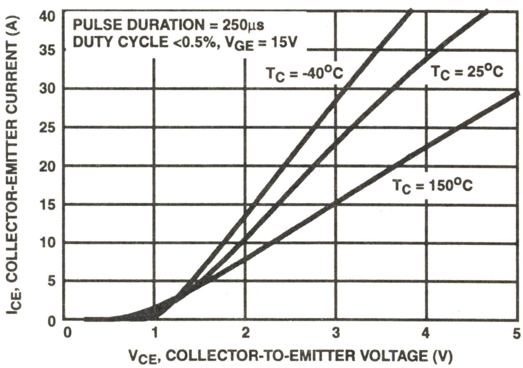


FIGURE 4. COLLECTOR-EMITTER ON - STATE VOLTAGE

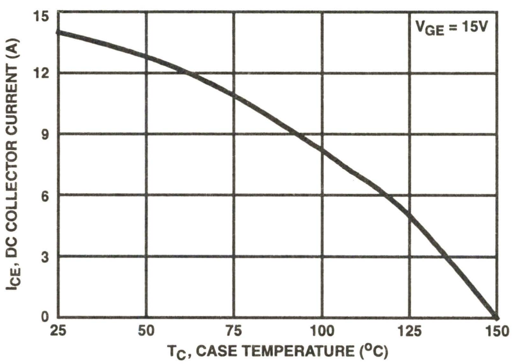


FIGURE 5. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

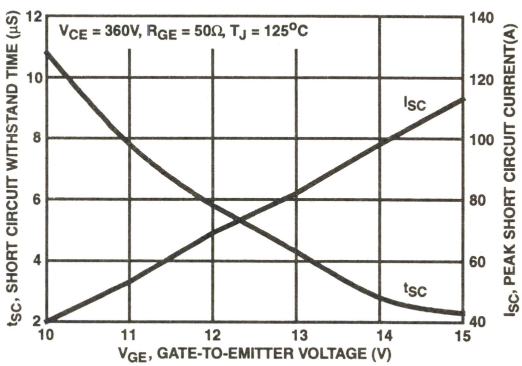


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

Typical Performance Curves (Continued)

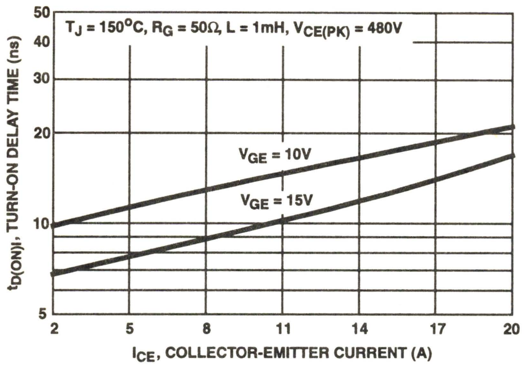


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

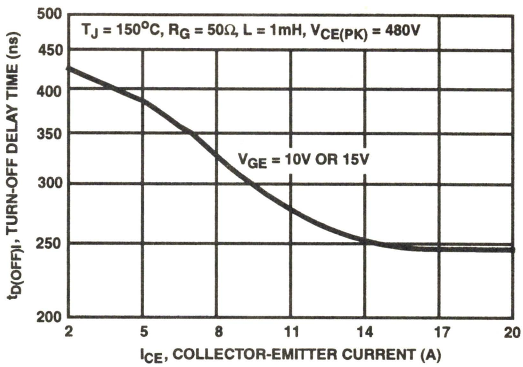


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

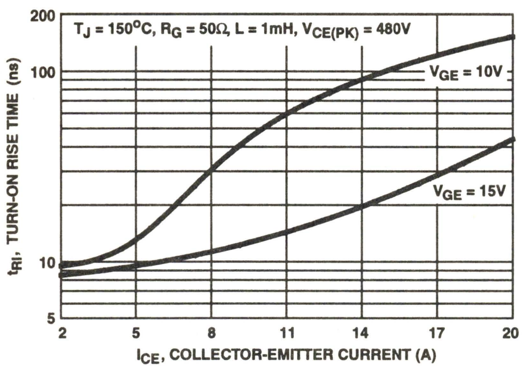


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

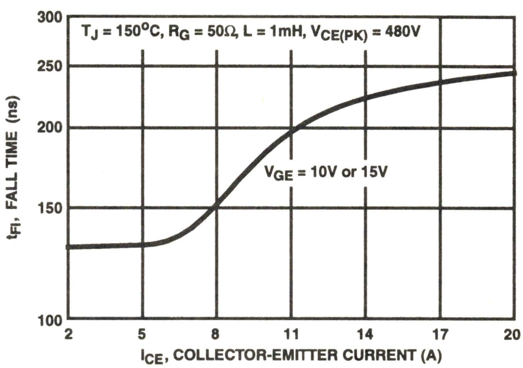


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

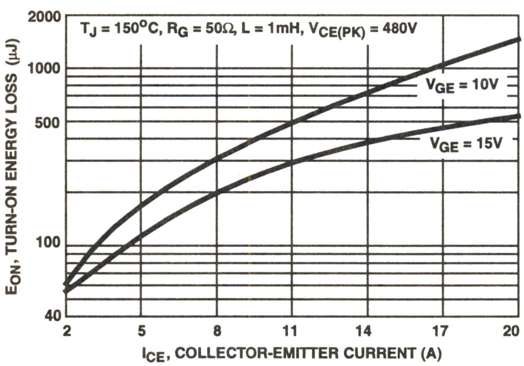


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

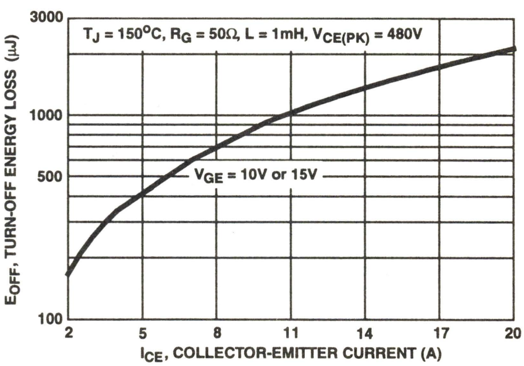


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

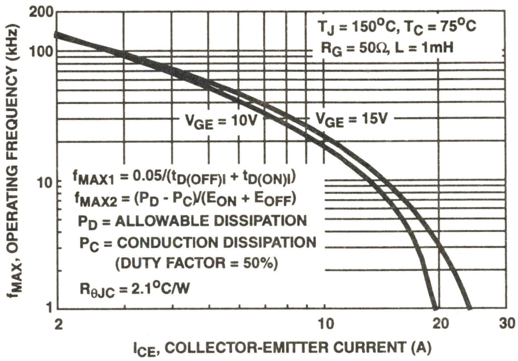


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

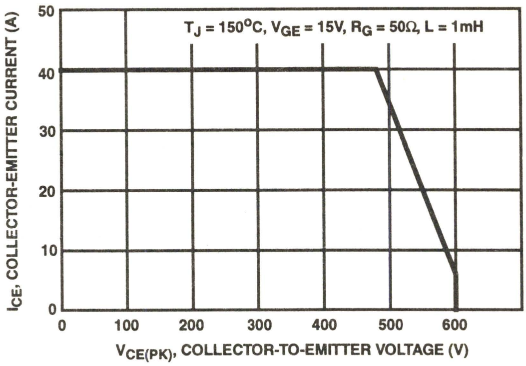


FIGURE 14. MINIMUM SWITCHING SAFE OPERATING AREA

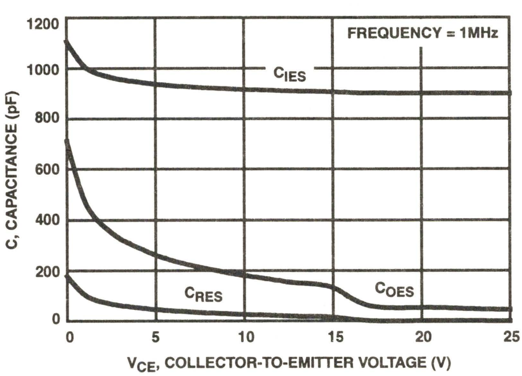


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

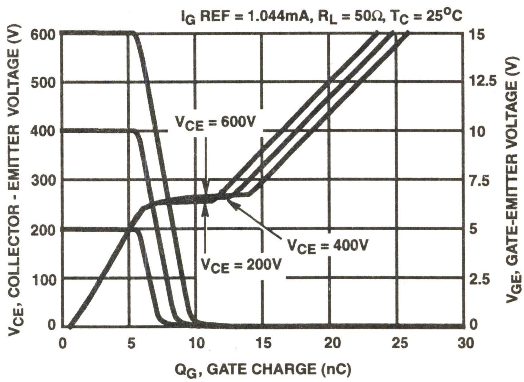


FIGURE 16. GATE CHARGE WAVEFORMS

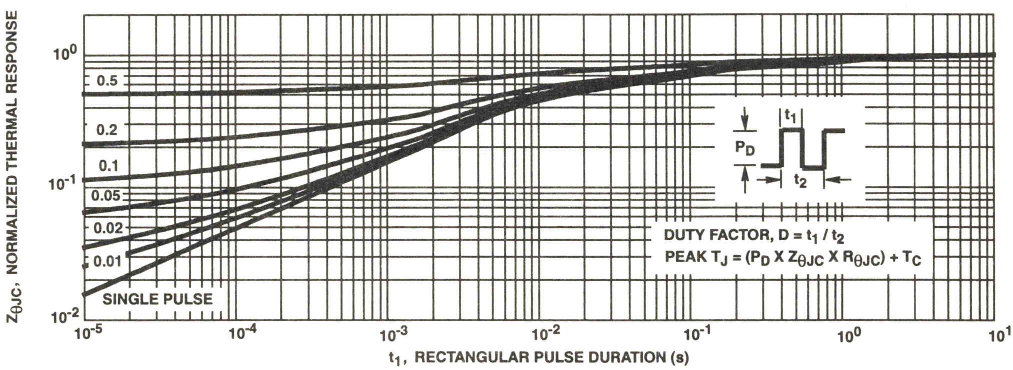


FIGURE 17. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Test Circuit and Waveform

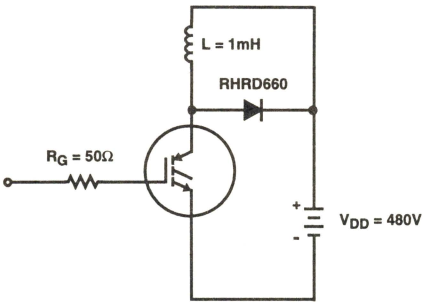


FIGURE 18. INDUCTIVE SWITCHING TEST CIRCUIT

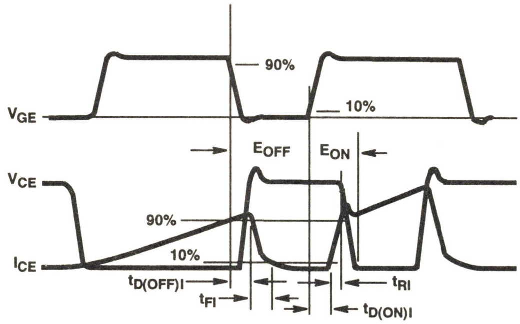


FIGURE 19. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

ECCOSORBD™ is a Trademark of Emerson and Cumming, Inc.

Operating Frequency Information

Operating Frequency Information for a Typical Device

Figure 13 is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 19.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$. E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 19. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

HARRIS SEMICONDUCTOR

HGTP7N60C3D, HGT1S7N60C3D, HGT1S7N60C3DS

14A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diodes

January 1997

Features

- 14A, 600V at $T_C = 25^oC$
- 600V Switching SOA Capability
- Typical Fall Time . . . . 140ns at $T_J = 150^oC$
- Short Circuit Rating
- Low Conduction Loss
- Hyperfast Anti-Parallel Diode

Description

The HGTP7N60C3D, HGT1S7N60C3D and HGT1S7N60C3DS are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25^oC and 150^oC. The IGBT used is developmental type TA49115. The diode used in anti-parallel with the IGBT is developmental type TA49057.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors

PACKAGING AVAILABILITY

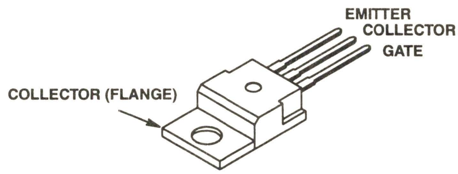
PART NUMBER	PACKAGE	BRAND
HGTP7N60C3D	TO-220AB	G7N60C3D
HGT1S7N60C3D	TO-262AA	G7N60C3D
HGT1S7N60C3DS	TO-263AB	G7N60C3D

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, i.e. HGT1S7N60C3DS9A.

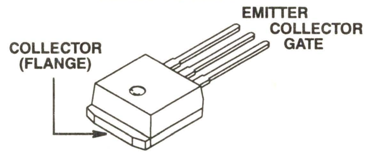
Formerly Developmental Type TA49121.

Packaging

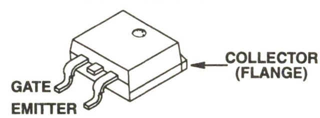
JEDEC TO-220AB



JEDEC TO-262AA

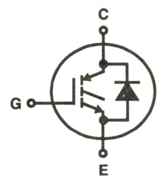


JEDEC TO-263AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTP7N60C3D, HGT1S7N60C3D HGT1S7N60C3DS	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	14	A
At $T_C = 110^oC$	I_{C110}	7	A
Average Diode Forward Current at 110^oC	$I_{(AVG)}$	8	A
Collector Current Pulsed (Note 1)	I_{CM}	56	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Figure 14	SSOA	40A at 480V	
Power Dissipation Total at $T_C = 25^oC$	P_D	60	W
Power Dissipation Derating $T_C > 25^oC$		0.487	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	^oC
Maximum Lead Temperature for Soldering	T_L	260	^oC
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	1	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	8	µs

NOTE:
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = 125^oC$, $R_{GE} = 50\Omega$.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	μA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	2.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.6	2.0	V
			$T_C = 150^oC$	-	1.9	2.4	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.0	5.0	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 25V$		-	-	±250	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 50\Omega$, $V_{GE} = 15V$, $L = 1mH$	$V_{CE(PK)} = 480V$	40	-	-	A
			$V_{CE(PK)} = 600V$	6	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	23	30	nC
			$V_{GE} = 20V$	-	30	38	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 50\Omega$, $L = 1mH$		-	8.5	-	ns
Current Rise Time	t_{RI}			-	11.5	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	350	400	ns
Current Fall Time	t_{FI}			-	140	275	ns
Turn-On Energy	E_{ON}			-	165	-	μJ
Turn-Off Energy (Note 3)	E_{OFF}			-	600	-	μJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 7A$		-	1.9	2.5	V
Diode Reverse Recovery Time	t_{rr}	$I_{EC} = 7A$, $dI_{EC}/dt = 200A/\mu s$		-	25	35	ns
		$I_{EC} = 1A$, $dI_{EC}/dt = 200A/\mu s$		-	18	30	ns
Thermal Resistance	$R_{\theta JC}$	IGBT		-	-	2.1	$^oC/W$
		Diode		-	-	2.0	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTP7N60C3D, HGT1S7N60C3D, and HGT1S7N60C3DS were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

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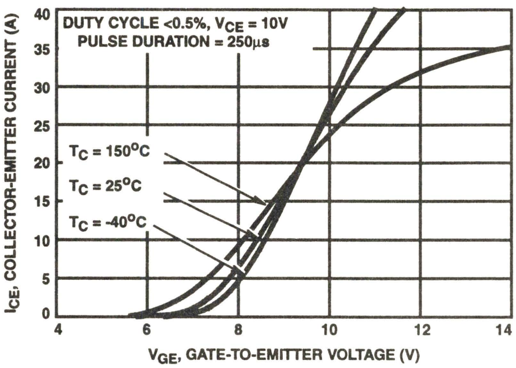
Typical Performance Curves



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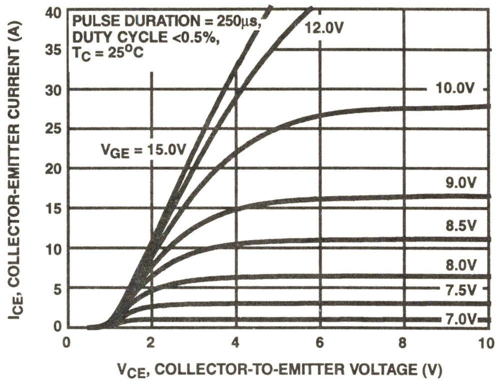
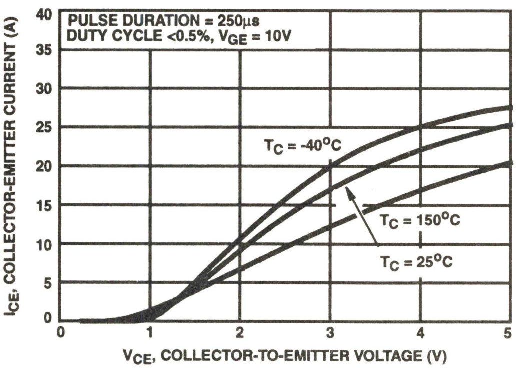


FIGURE 2. SATURATION CHARACTERISTICS



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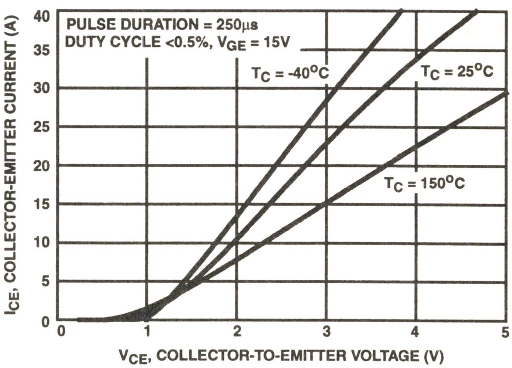

FIGURE 4. COLLECTOR-EMITTER ON - STATE VOLTAGE

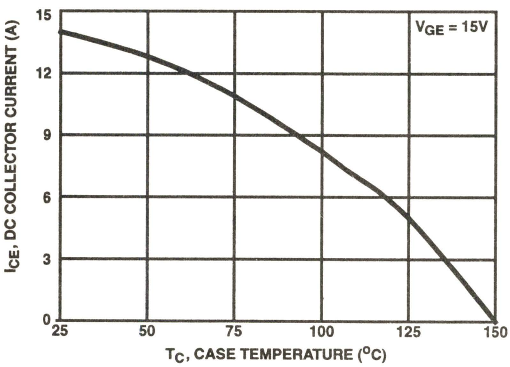

FIGURE 5. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

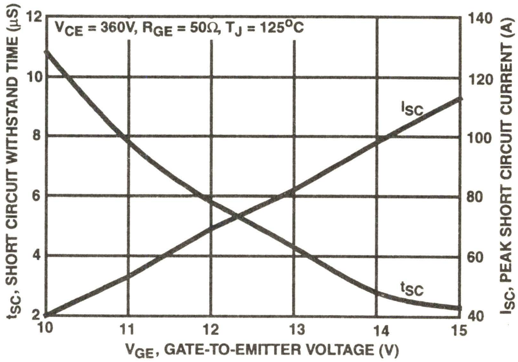

FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

Typical Performance Curves (Continued)

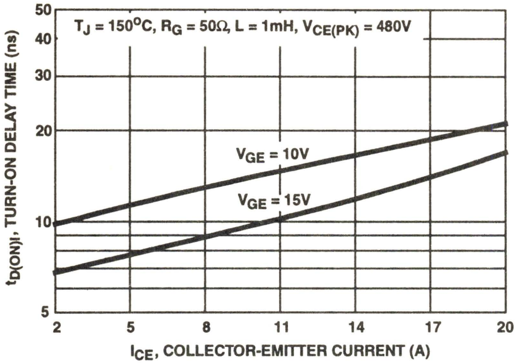

FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

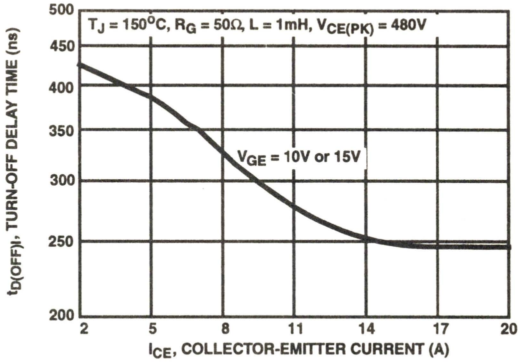

FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

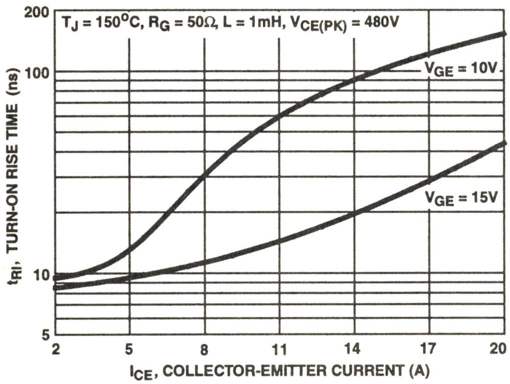

FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

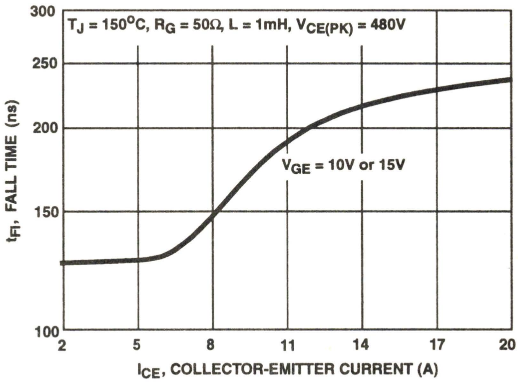

FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

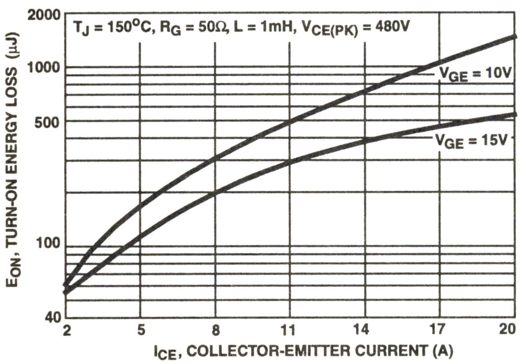

FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

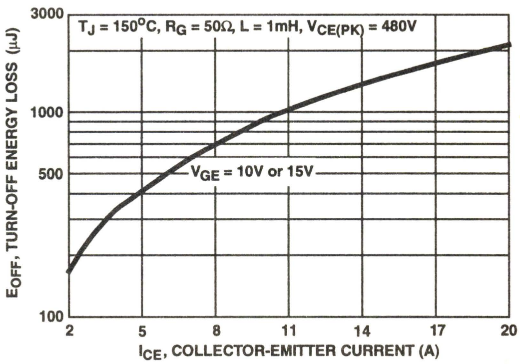

FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

3
C-SPEED UFS SERIES

Typical Performance Curves (Continued)

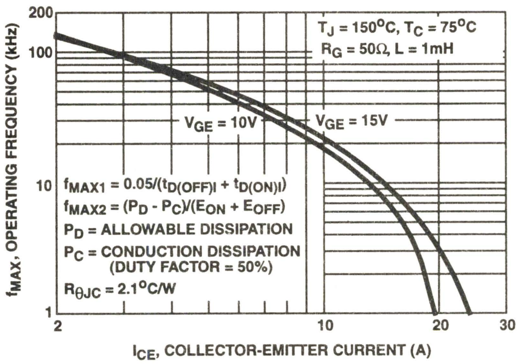

FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

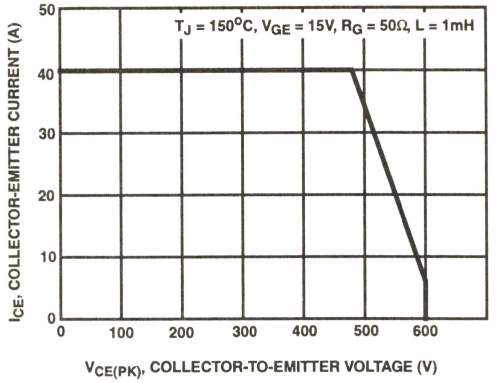

FIGURE 14. MINIMUM SWITCHING SAFE OPERATING AREA

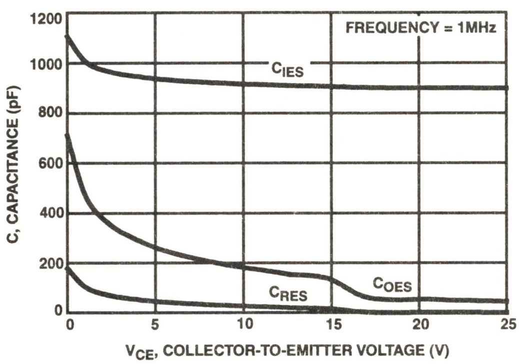

FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

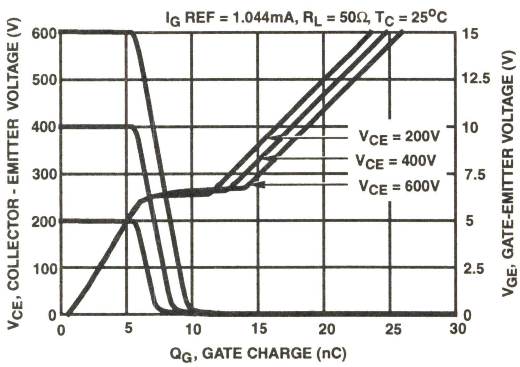

FIGURE 16. GATE CHARGE WAVEFORMS

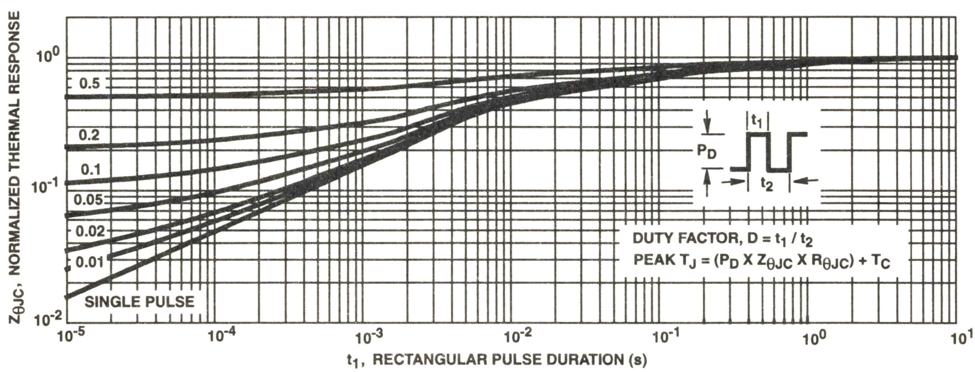

FIGURE 17. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Typical Performance Curves (Continued)

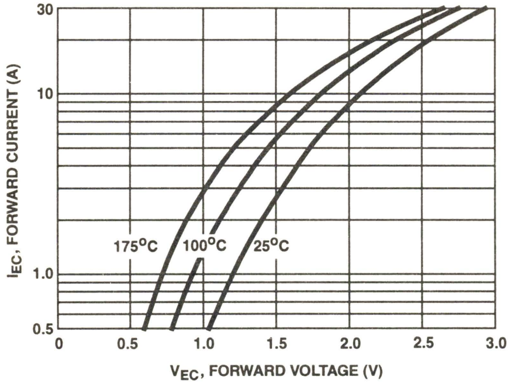

FIGURE 18. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

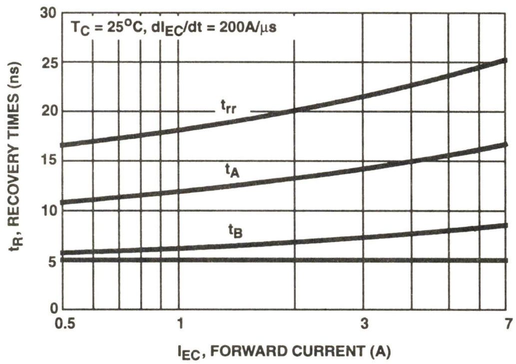

FIGURE 19. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveform

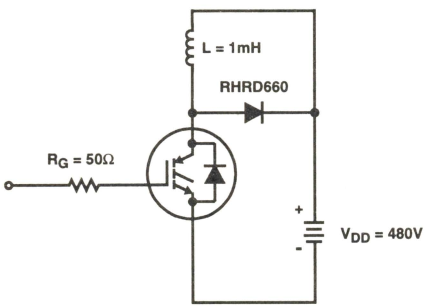

FIGURE 20. INDUCTIVE SWITCHING TEST CIRCUIT

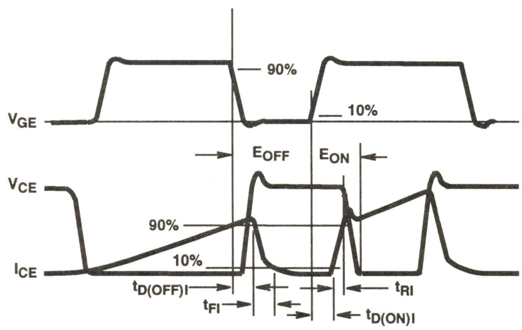

FIGURE 21. SWITCHING TEST WAVEFORMS

3

C-SPEED UFS SERIES

Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 21.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

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Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

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2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.

ECCOSORBD™ LD26 is a Trademark of Emerson and Cumming, Inc.

3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

HGTP12N60C3, HGT1S12N60C3, HGT1S12N60C3S

January 1997

24A, 600V, UFS Series N-Channel IGBTs

Features

- 24A, 600V at $T_C = 25^oC$
- 600V Switching SOA Capability
- Typical Fall Time . . . . 230ns at $T_J = 150^oC$
- Short Circuit Rating
- Low Conduction Loss

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTP12N60C3	TO-220AB	P12N60C3
HGT1S12N60C3	TO-262AA	S12N60C3
HGT1S12N60C3S	TO-263AB	S12N60C3

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in Tape and Reel, i.e., HGT1S12N60C3S9A.

Formerly Developmental Type TA49123.

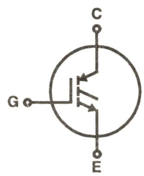
Description

The HGTP12N60C3, HGT1S12N60C3 and HGT1S12N60C3S are MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25^{o}C and 150^{o}C.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

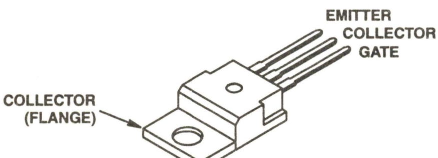
Terminal Diagram

N-CHANNEL ENHANCEMENT MODE

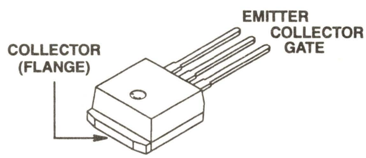


Packaging

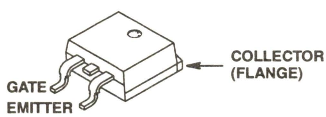
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTP12N60C3, HGT1S12N60C3, HGT1S12N60C3S	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	24	A
At $T_C = 110^oC$	I_{C110}	12	A
Collector Current Pulsed (Note 1)	I_{CM}	96	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Figure 14	SSOA	24A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	104	W
Power Dissipation Derating $T_C > 25^oC$		0.83	W/^{o}C
Reverse Voltage Avalanche Energy	E_{ARV}	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	4	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	13	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = 125^oC$, $R_{GE} = 25\Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$, $V_{GE} = 0V$		24	30	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	1.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.65	2.0	V
			$T_C = 150^oC$	-	1.85	2.2	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.0	5.0	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 25\Omega$, $V_{GE} = 15V$, $L = 100\mu H$	$V_{CE(PK)} = 480V$	80	-	-	A
			$V_{CE(PK)} = 600V$	24	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	7.6	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	48	55	nC
			$V_{GE} = 20V$	-	62	71	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 25\Omega$, $L = 100\mu H$		-	14	-	ns
Current Rise Time	t_{RI}			-	16	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	270	400	ns
Current Fall Time	t_{FI}			-	210	275	ns
Turn-On Energy	E_{ON}			-	380	-	µJ
Turn-Off Energy (Note 3)	E_{OFF}			-	900	-	µJ
Thermal Resistance	$R_{\theta JC}$			-	-	1.2	^{o}C/W

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTP12N60C3, HGT1S12N60C3 and HGT1S12N60C3S were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

Typical Performance Curves

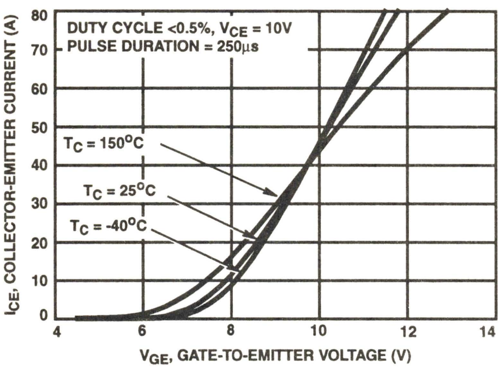


FIGURE 1. TRANSFER CHARACTERISTICS

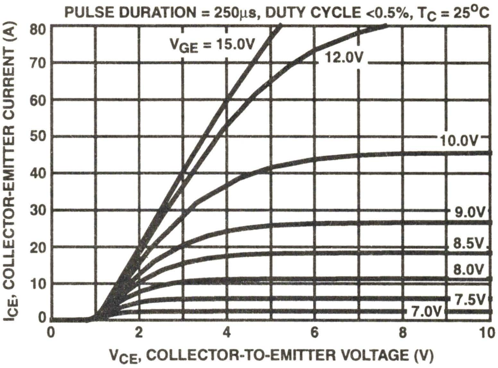


FIGURE 2. SATURATION CHARACTERISTICS

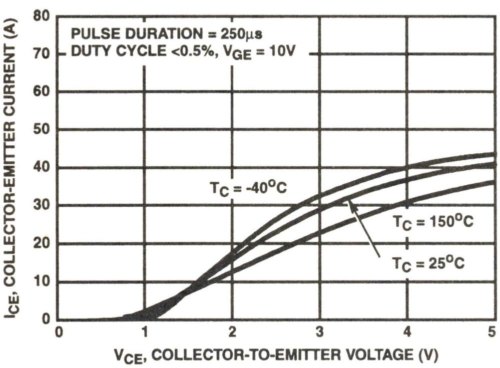


FIGURE 3. COLLECTOR-EMITTER ON-STATE VOLTAGE

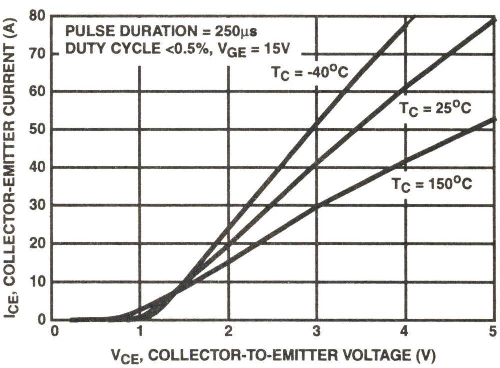


FIGURE 4. COLLECTOR-EMITTER ON-STATE VOLTAGE

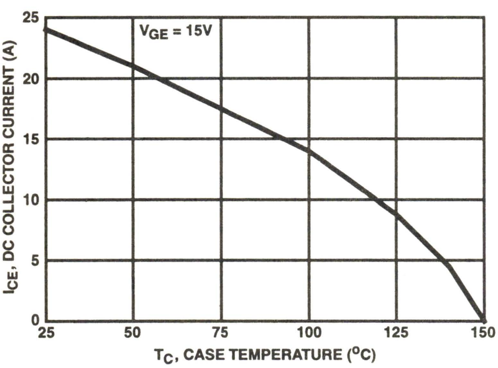


FIGURE 5. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

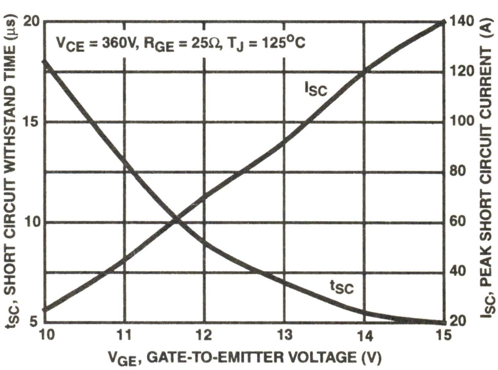


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

Typical Performance Curves (Continued)

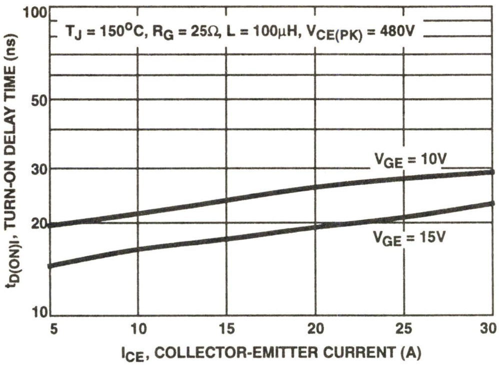


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

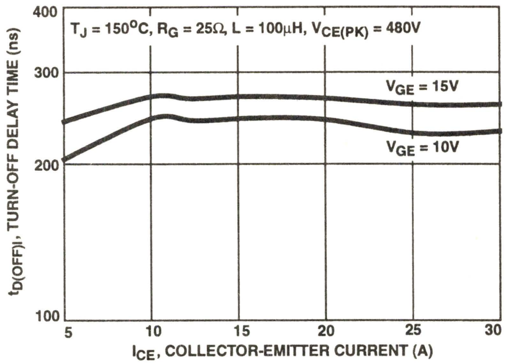


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

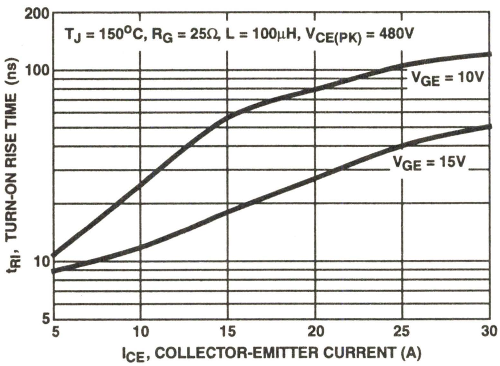


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

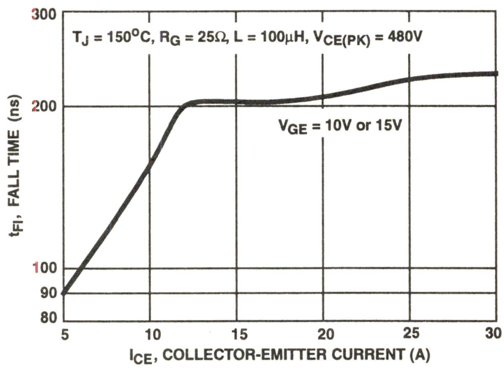


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

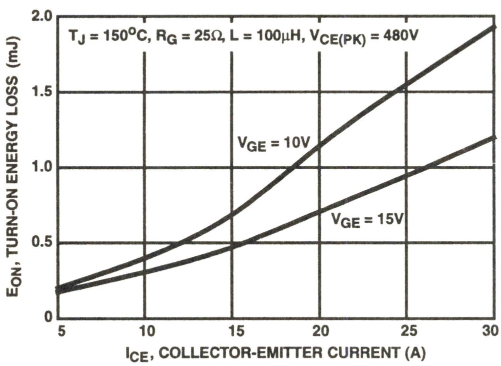


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

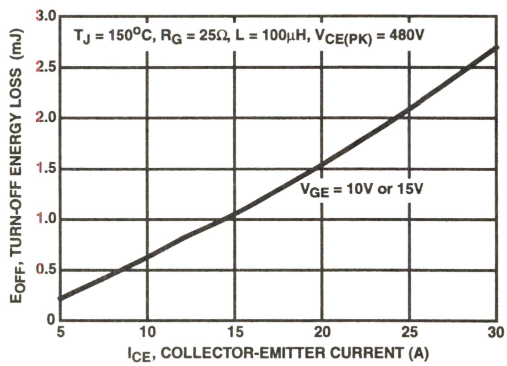
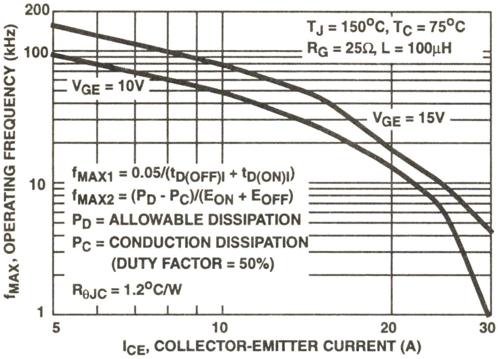


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)



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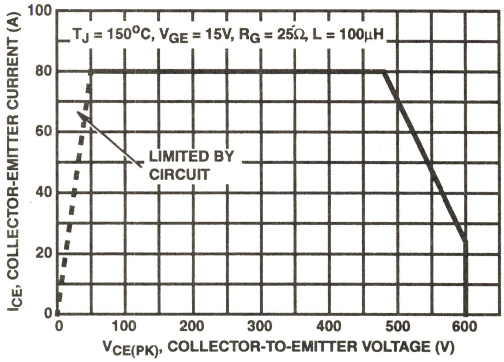

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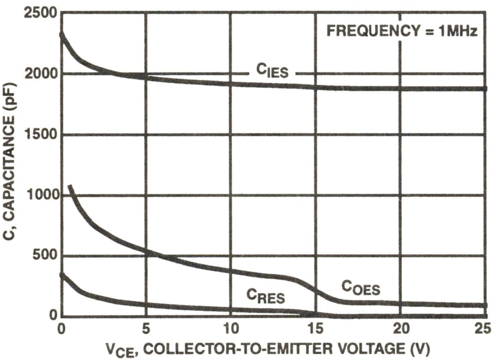

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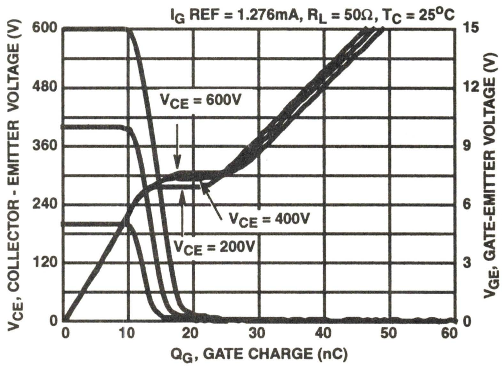

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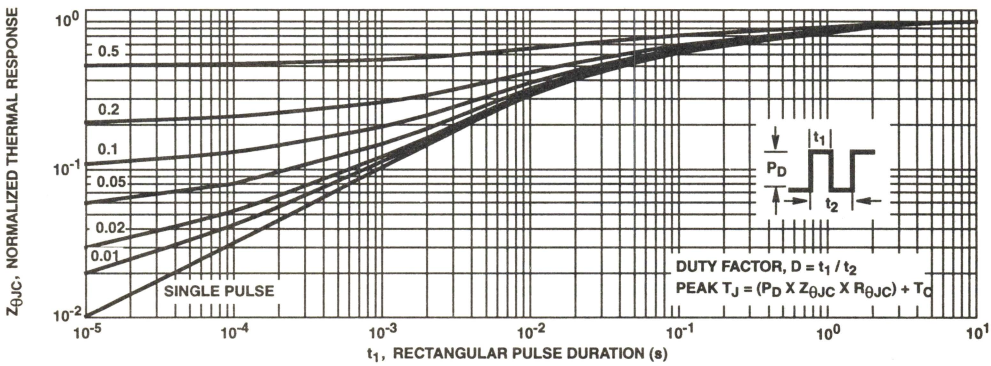

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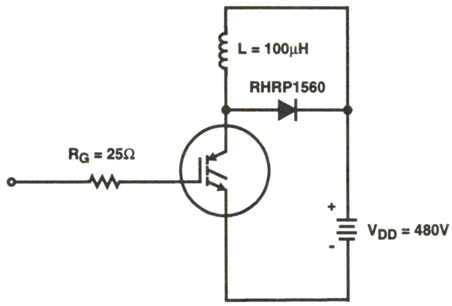

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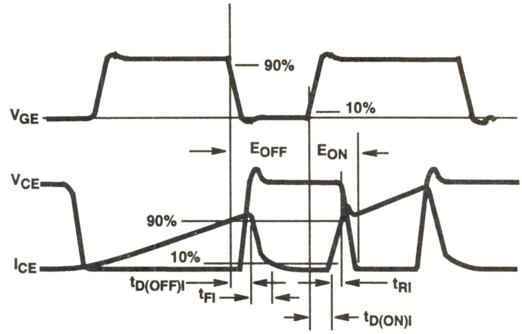

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7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

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f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

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HARRIS SEMICONDUCTOR HGTG12N60C3D

24A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode

January 1997

Features

- 24A, 600V at $T_C = 25^oC$
- Typical Fall Time . . . . 210ns at $T_J = 150^oC$
- Short Circuit Rating
- Low Conduction Loss
- Hyperfast Anti-Parallel Diode

Description

The HGTG12N60C3D is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C. The IGBT used is the development type TA49123. The diode used in antiparallel with the IGBT is the development type TA49061.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential.

PACKAGING AVAILABILITY

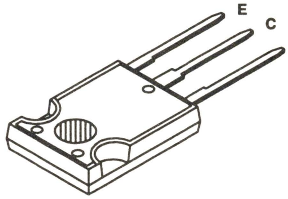
PART NUMBER	PACKAGE	BRAND
HGTG12N60C3D	TO-247	G12N60C3D

NOTE: When ordering, use the entire part number.

Formerly Developmental Type TA49117.

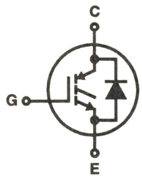
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



3

C-SPEED UFS SERIES

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTG12N60C3D	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	24	A
At $T_C = 110^oC$	I_{C110}	12	A
Average Diode Forward Current at 110°C	$I_{(AVG)}$	15	A
Collector Current Pulsed (Note 1)	I_{CM}	96	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$	SSOA	24A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	104	W
Power Dissipation Derating $T_C > 25^oC$		0.83	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	4	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	13	µs

NOTE:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = 125^oC$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number 4043.1

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$, $V_{GE} = 0V$		15	25	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	2.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.65	2.0	V
			$T_C = 150^oC$	-	1.85	2.2	V
		$I_C = 15A$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.80	2.2	V
			$T_C = 150^oC$	-	2.0	2.4	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.0	5.0	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA	SSOA	$T_J = 150^oC$, $V_{GE} = 15V$, $R_G = 25\Omega$, $L = 100\mu H$	$V_{CE(PK)} = 480V$	80	-	-	A
			$V_{CE(PK)} = 600V$	24	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	7.6	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	48	55	nC
			$V_{GE} = 20V$	-	62	71	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 25\Omega$, $L = 100\mu H$		-	14	-	ns
Current Rise Time	t_{RI}			-	16	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	270	400	ns
Current Fall Time	t_{FI}			-	210	275	ns
Turn-On Energy	E_{ON}			-	380	-	µJ
Turn-Off Energy (Note 3)	E_{OFF}			-	900	-	µJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 12A$		-	1.7	2.0	V
Diode Reverse Recovery Time	t_{rr}	$I_{EC} = 12A$, $dI_{EC}/dt = 100A/\mu s$		-	34	42	ns
		$I_{EC} = 1.0A$, $dI_{EC}/dt = 100A/\mu s$		-	30	37	ns
Thermal Resistance	$R_{\theta JC}$	IGBT		-	-	1.2	$^oC/W$
		Diode		-	-	1.5	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse, and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTG12N60C3D was tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

Typical Performance Curves

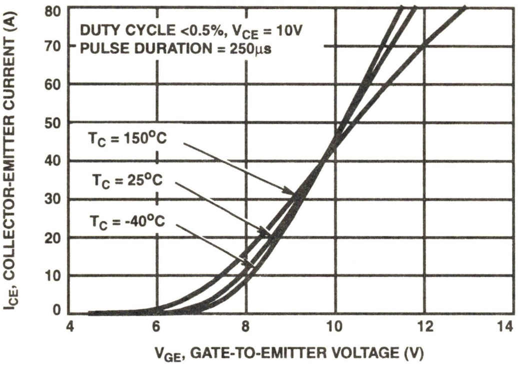


FIGURE 1. TRANSFER CHARACTERISTICS

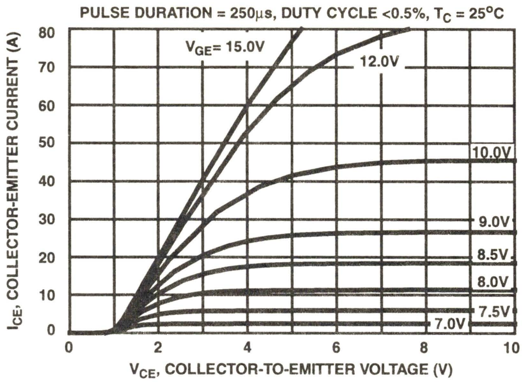


FIGURE 2. SATURATION CHARACTERISTICS

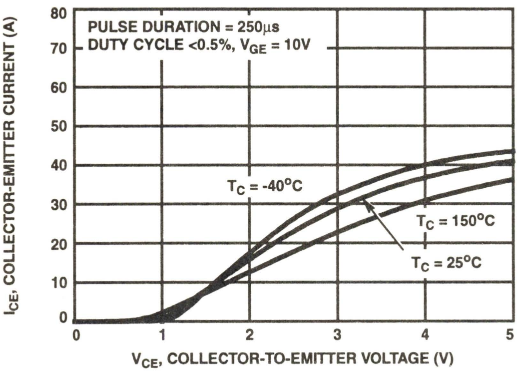


FIGURE 3. COLLECTOR-EMITTER ON-STATE VOLTAGE

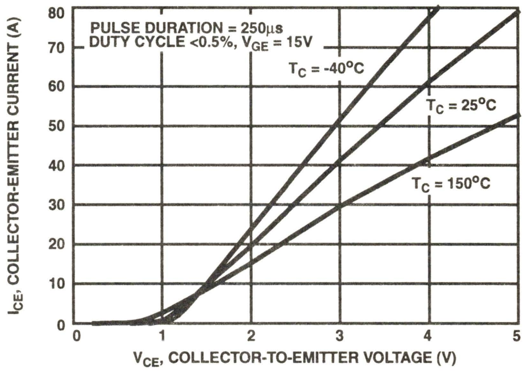


FIGURE 4. COLLECTOR-EMITTER ON-STATE VOLTAGE

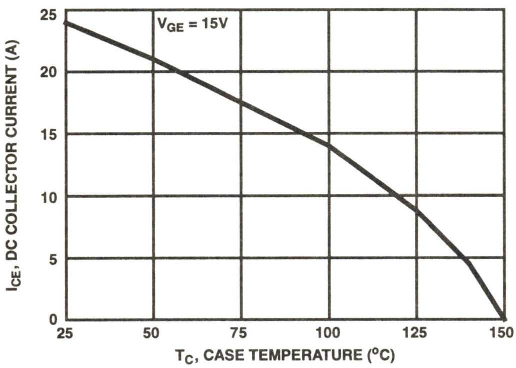


FIGURE 5. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

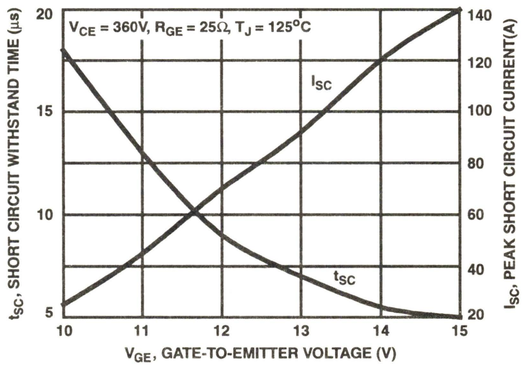


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

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C-SPEED UFS SERIES

Typical Performance Curves (Continued)

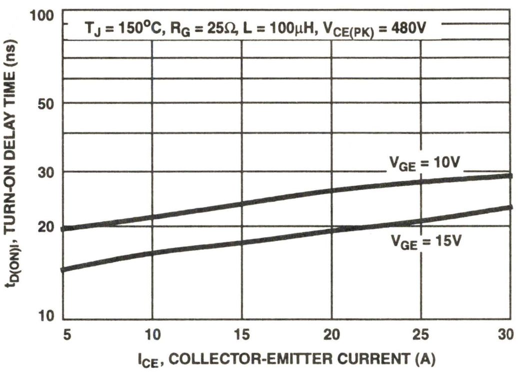


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

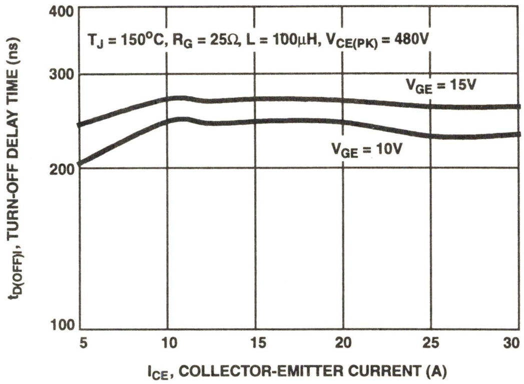


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

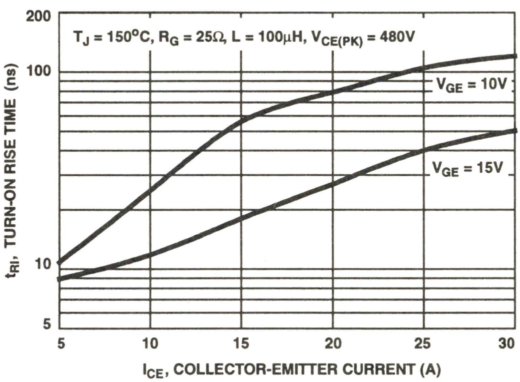


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

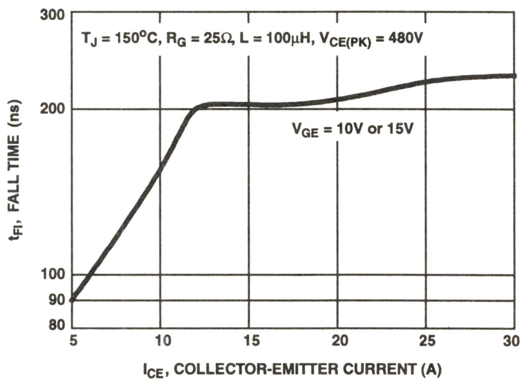


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

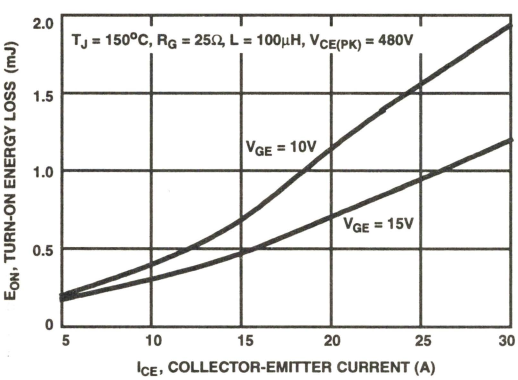


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

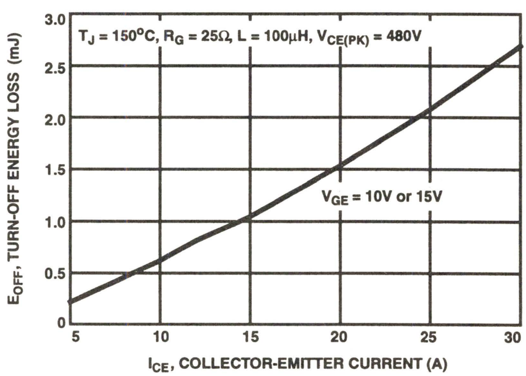


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

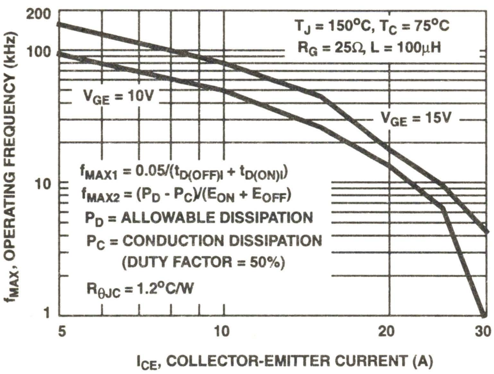


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

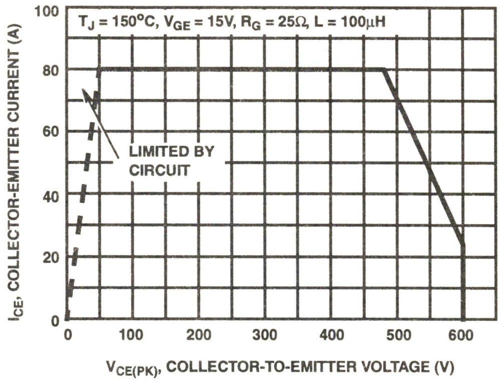


FIGURE 14. SWITCHING SAFE OPERATING AREA

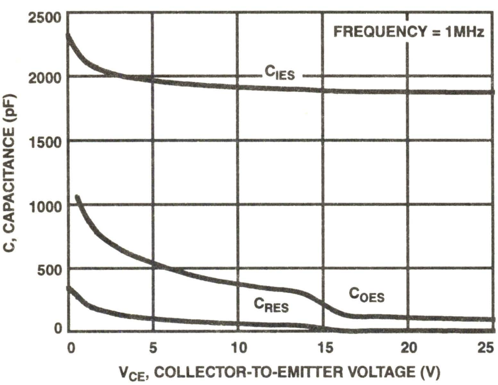
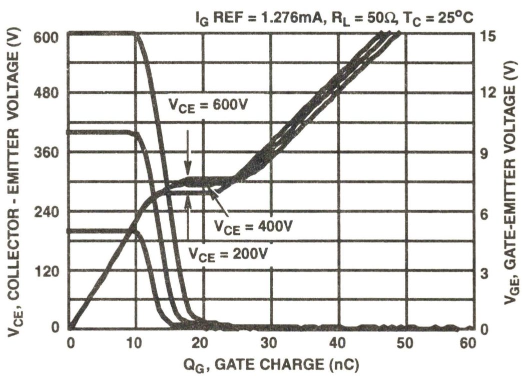


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE



FIGUE 16. GATE CHARGE WAVEFORMS

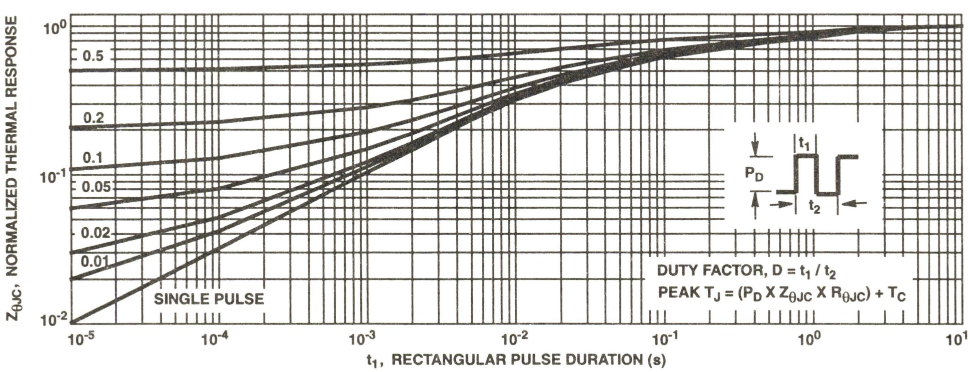


FIGURE 17. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

3
C-SPEED
UFS SERIES

Typical Performance Curves (Continued)

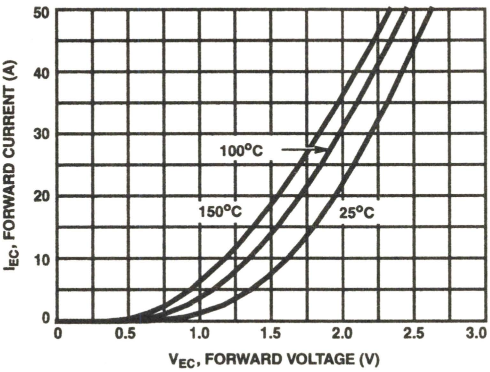


FIGURE 18. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

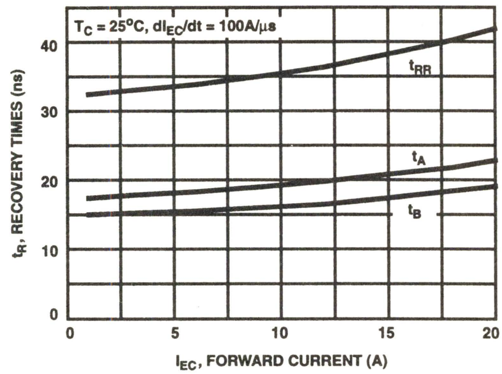


FIGURE 19. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveform

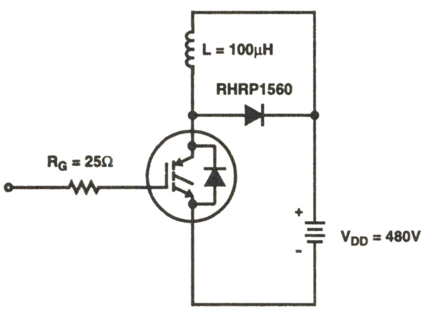


FIGURE 20. INDUCTIVE SWITCHING TEST CIRCUIT

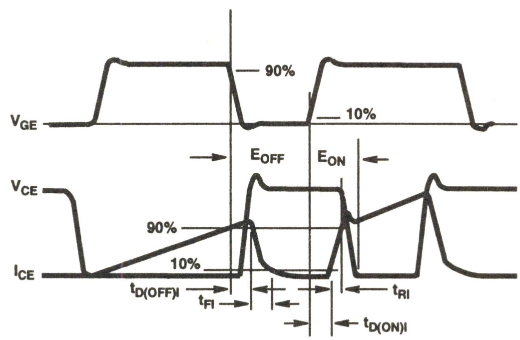


FIGURE 21. SWITCHING TEST WAVEFORMS

Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 21.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 21. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBT's are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener Diode from gate to emitter. If gate protection is required an external Zener is recommended.

HARRIS SEMICONDUCTOR

HGTP12N60C3D, HGT1S12N60C3D, HGT1S12N60C3DS

24A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diodes

January 1997

Features

- 24A, 600V at $T_C = 25^oC$
- Typical Fall Time at $T_J = 150^oC$ 210ns
- Short Circuit Rating
- Low Conduction Loss
- Hyperfast Anti-Parallel Diode

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTP12N60C3D	TO-220AB	12N60C3D
HGT1S12N60C3D	TO-262AA	12N60C3D
HGT1S12N60C3DS	TO-263AB	12N60C3D

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263 variant in Tape and Reel, i.e., HGT1S12N60C3DS9A.

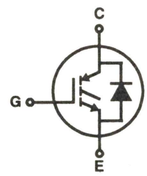
Description

This family of MOS gated high voltage switching devices combine the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C. The IGBT used is the development type TA49123. The diode used in anti-parallel with the IGBT is the development type TA49188.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential.

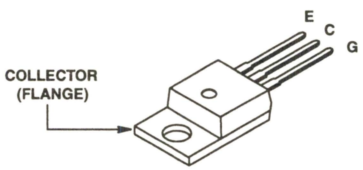
Formerly Developmental Type TA49182.

Symbol

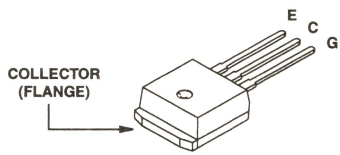


Packaging

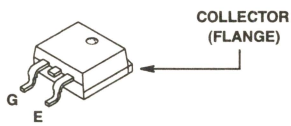
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,53	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4261**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		ALL TYPES	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	24	A
At $T_C = 110^oC$	I_{C110}	12	A
Average Diode Forward Current at 110^oC	$I_{(AVG)}$	12	A
Collector Current Pulsed (Note 1)	I_{CM}	96	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Figure 14	SSOA	24A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	104	W
Power Dissipation Derating $T_C > 25^oC$		0.83	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	4	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	13	µs

NOTE:
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = 125^oC$, $R_{GE} = 25\Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
			$T_C = 150^oC$	-	-	2.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.65	2.0	V
			$T_C = 150^oC$	-	1.85	2.2	V
		$I_C = 15A$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.80	2.2	V
			$T_C = 150^oC$	-	2.0	2.4	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$		3.0	5.0	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA	SSOA	$T_J = 150^oC$, $V_{GE} = 15V$, $R_G = 25\Omega$, $L = 100\mu H$	$V_{CE(PK)} = 480V$	80	-	-	A
			$V_{CE(PK)} = 600V$	24	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	7.6	-	V
On-State Gate Charge	$Q_{g(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	48	55	nC
			$V_{GE} = 20V$	-	62	71	nC
Current Turn-On Delay Time	$t_{d(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 25\Omega$, $L = 100\mu H$ Note 3		-	28	-	ns
Current Rise Time	t_{ri}			-	20	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$			-	270	400	ns
Current Fall Time	t_{fi}			-	210	275	ns
Turn-On Energy	E_{ON}			-	380	-	µJ
Turn-Off Energy (Note 3)	E_{OFF}			-	900	-	µJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 12A$		-	1.7	2.1	V

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Diode Reverse Recovery Time	t_{rr}	I_{EC} = 12A, dI_{EC}/dt = 200A/μs	-	32	40	ns
		I_{EC} = 1.0A, dI_{EC}/dt = 200A/μs	-	23	30	ns
Thermal Resistance	$R_{\theta JC}$	IGBT	-	-	1.2	$^oC/W$
		Diode	-	-	1.9	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse, and ending at the point where the collector current equals zero (I_{CE} = 0A). This family of devices was tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include losses due to diode recovery.

Typical Performance Curves

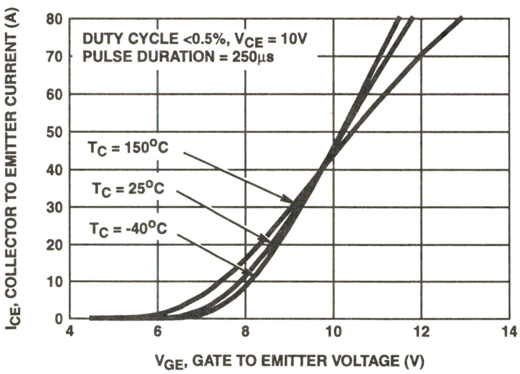


FIGURE 1. TRANSFER CHARACTERISTICS

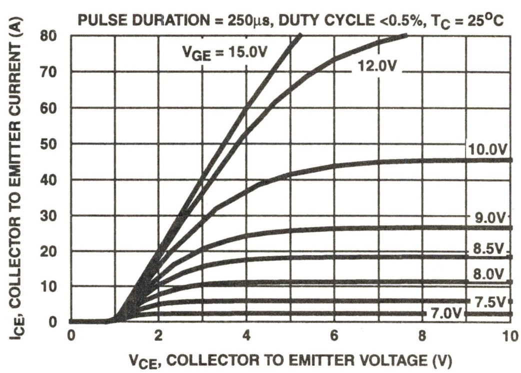


FIGURE 2. SATURATION CHARACTERISTICS

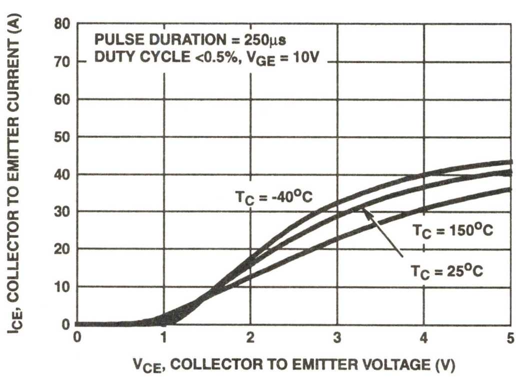


FIGURE 3. COLLECTOR TO EMITTER ON-STATE VOLTAGE

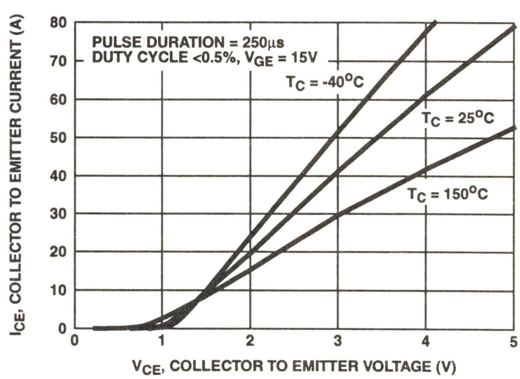


FIGURE 4. COLLECTOR TO EMITTER ON-STATE VOLTAGE

Typical Performance Curves (Continued)

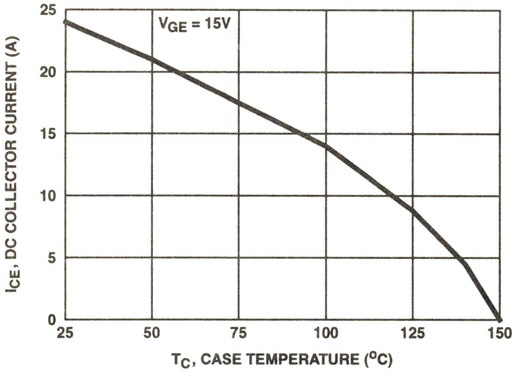


FIGURE 5. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

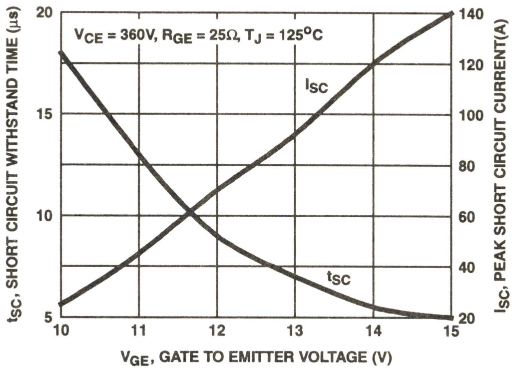


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

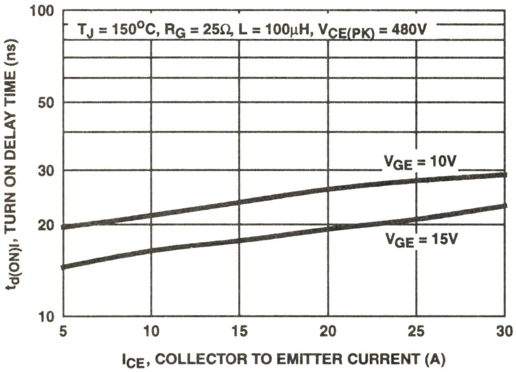


FIGURE 7. TURN ON DELAY TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

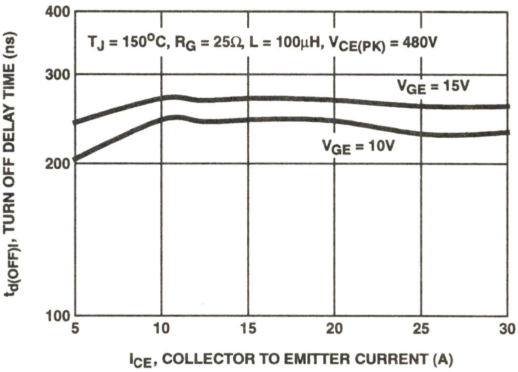


FIGURE 8. TURN OFF DELAY TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

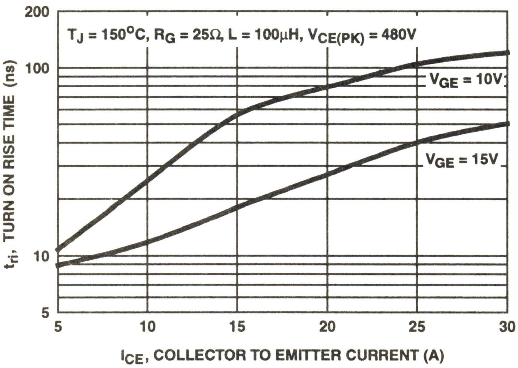


FIGURE 9. TURN ON RISE TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

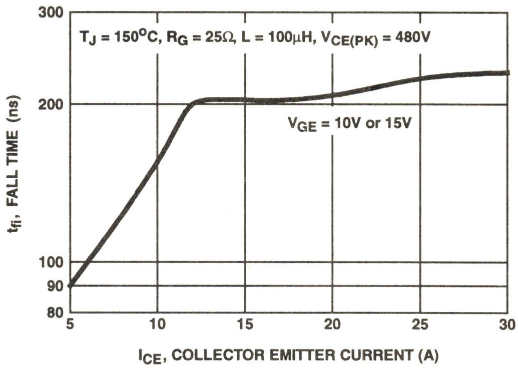


FIGURE 10. TURN OFF FALL TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

3

C-SPEED UFS SERIES

Typical Performance Curves (Continued)

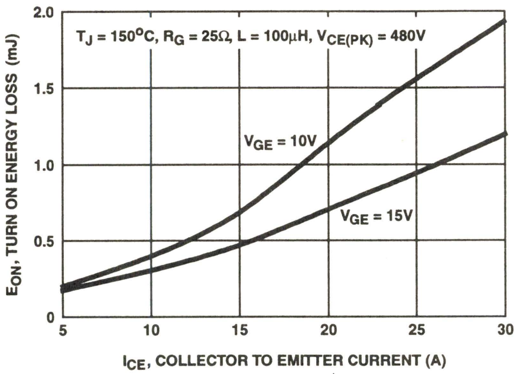


FIGURE 11. TURN ON ENERGY LOSS AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

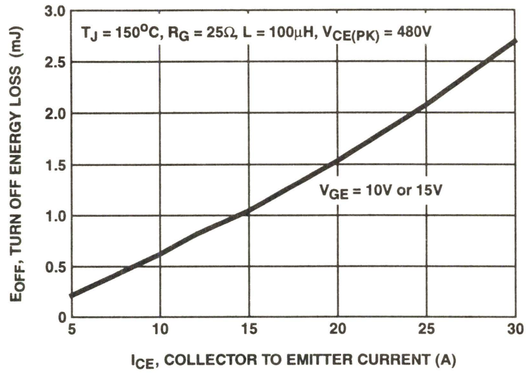


FIGURE 12. TURN OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

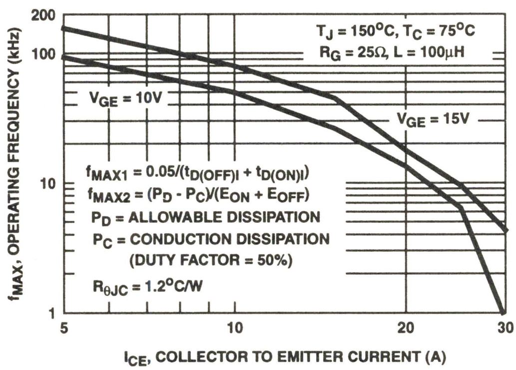


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

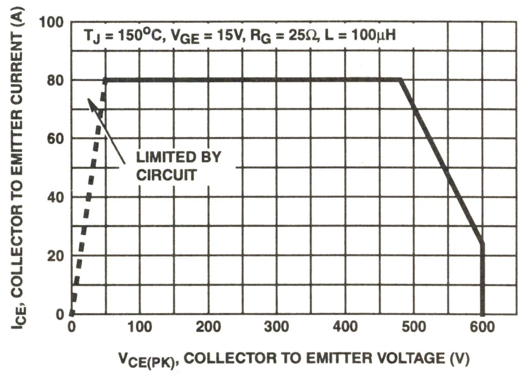


FIGURE 14. SWITCHING SAFE OPERATING AREA

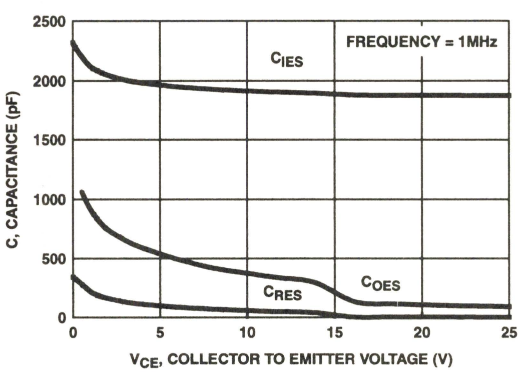


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR TO EMITTER VOLTAGE

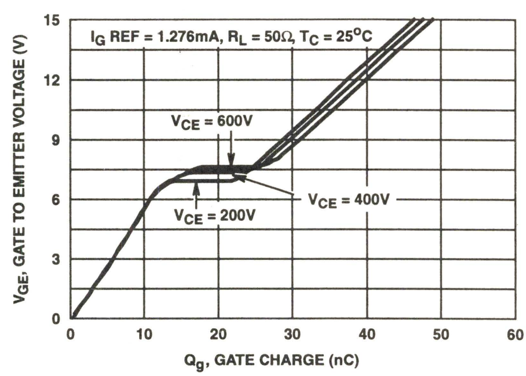


FIGURE 16. GATE CHARGE WAVEFORMS

Typical Performance Curves (Continued)

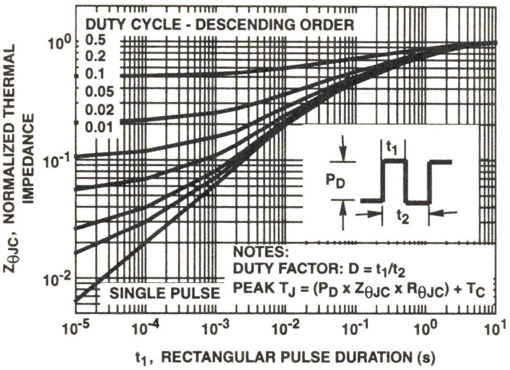


FIGURE 17. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

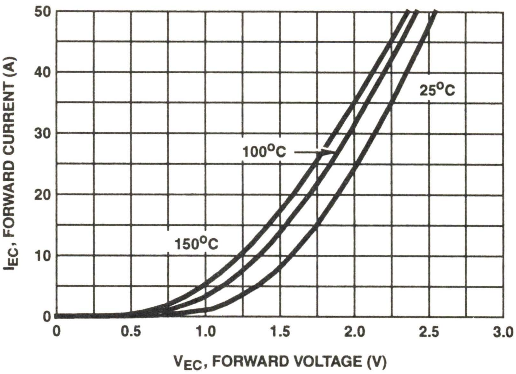


FIGURE 18. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

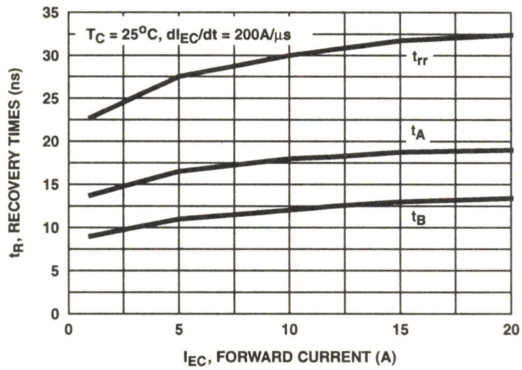


FIGURE 19. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveform

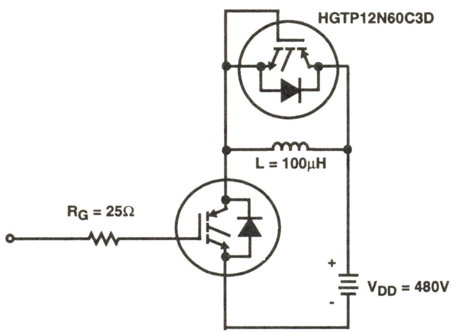


FIGURE 20. INDUCTIVE SWITCHING TEST CIRCUIT

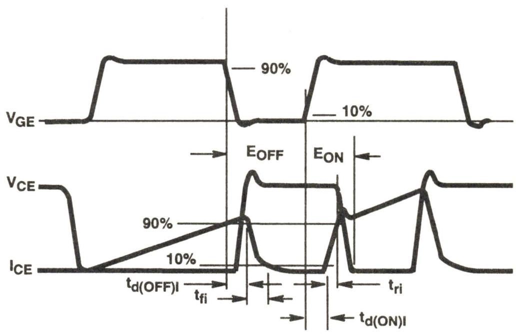


FIGURE 21. SWITCHING TEST WAVEFORMS

Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 21.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 21. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$).

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBT's are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener Diode from gate to emitter. If gate protection is required, an external Zener is recommended.

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HGTG30N60C3

January 1997

63A, 600V, UFS Series N-Channel IGBT

Features

- 63A, 600V at $T_C = 25^oC$
- 600V Switching SOA Capability
- Typical Fall Time . . . . 230ns at $T_J = 150^oC$
- Short Circuit Rating
- Low Conduction Loss

Description

The HGTG30N60C3 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

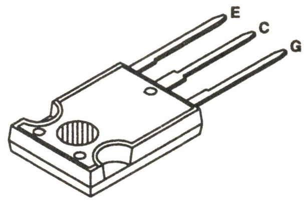
PART NUMBER	PACKAGE	BRAND
HGTG30N60C3	TO-247	G30N60C3

NOTE: When ordering, use the entire part number.

Formerly Developmental Type TA49051.

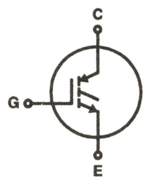
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTG30N60C3	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	63	A
At $T_C = 110^oC$	I_{C110}	30	A
Collector Current Pulsed (Note 1)	I_{CM}	252	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Figure 14	SSOA	60A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	208	W
Power Dissipation Derating $T_C > 25^oC$		1.67	W/°C
Reverse Voltage Avalanche Energy	E_{ARV}	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	4	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	15	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = 125^oC$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$, $V_{GE} = 0V$		15	25	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	2.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.5	1.8	V
			$T_C = 150^oC$	-	1.7	2.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.0	5.2	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 3\Omega$, $V_{GE} = 15V$, $L = 100\mu H$	$V_{CE(PK)} = 480V$	200	-	-	A
			$V_{CE(PK)} = 600V$	60	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8.1	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	162	180	nC
			$V_{GE} = 20V$	-	216	250	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 3\Omega$, $L = 100\mu H$		-	40	-	ns
Current Rise Time	t_{RI}			-	45	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	320	400	ns
Current Fall Time	t_{FI}			-	230	275	ns
Turn-On Energy	E_{ON}			-	1050	-	µJ
Turn-Off Energy (Note 3)	E_{OFF}			-	2500	-	µJ
Thermal Resistance	$R_{\theta JC}$			-	-	0.6	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTG30N60C3 was tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total turn-off energy loss. Turn-On losses include diode losses.

Typical Performance Curves

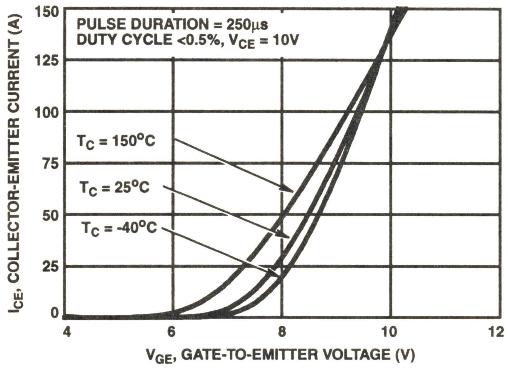


FIGURE 1. TRANSFER CHARACTERISTICS

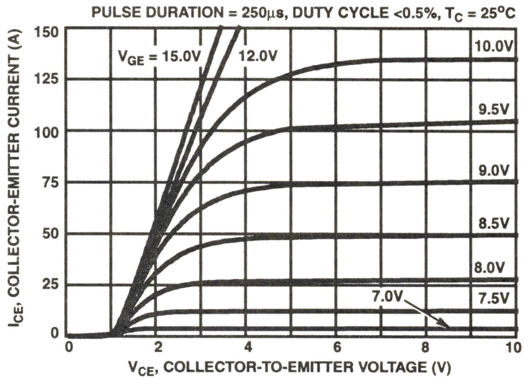


FIGURE 2. SATURATION CHARACTERISTICS

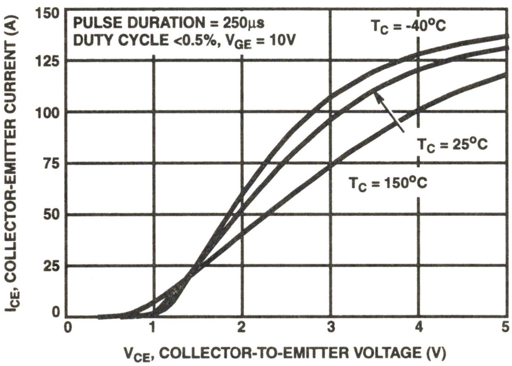


FIGURE 3. COLLECTOR-EMITTER ON-STATE VOLTAGE

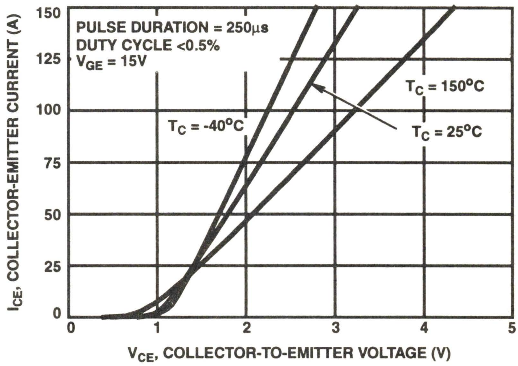


FIGURE 4. COLLECTOR-EMITTER ON-STATE VOLTAGE

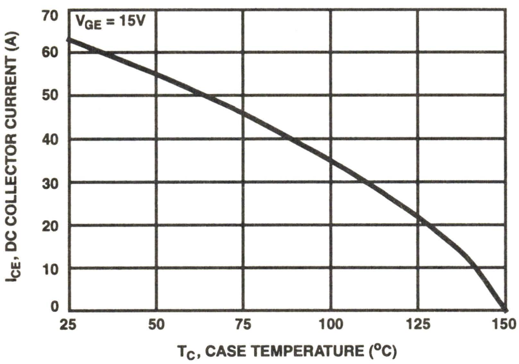


FIGURE 5. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

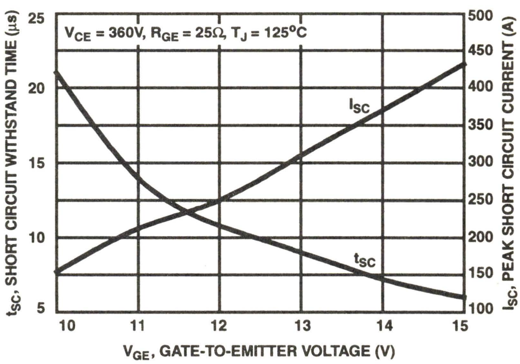


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

3
C-SPEED UFS SERIES

Typical Performance Curves (Continued)

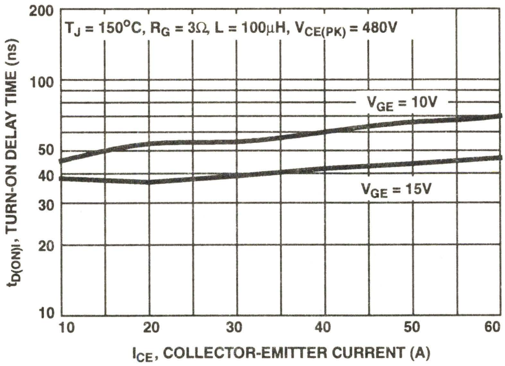


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

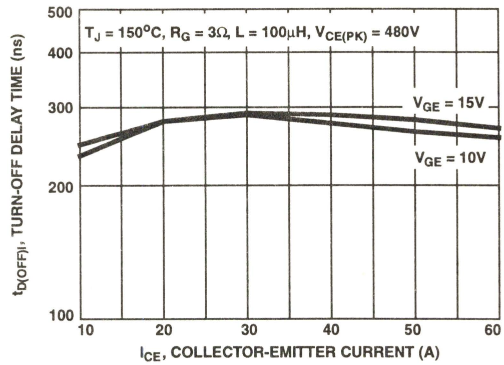


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

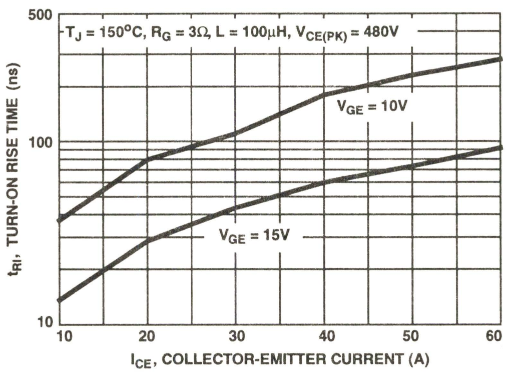


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

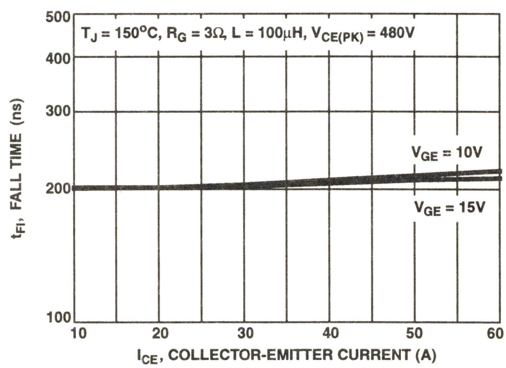


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

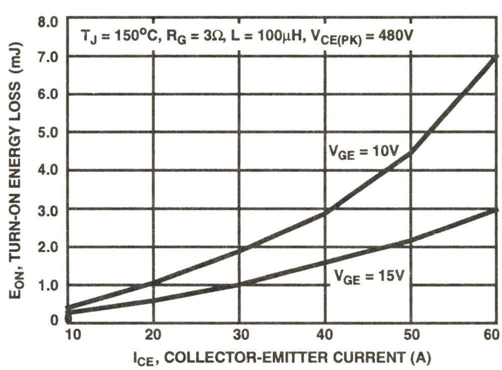


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

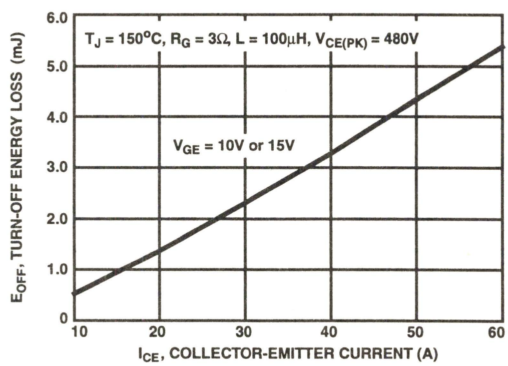


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

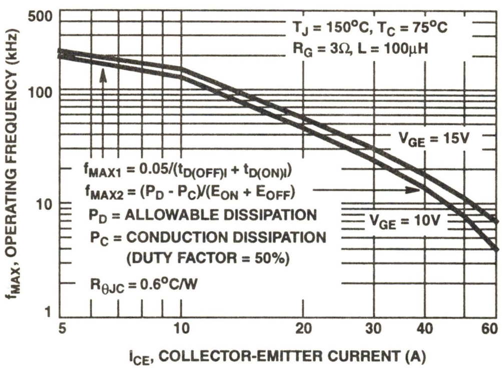


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

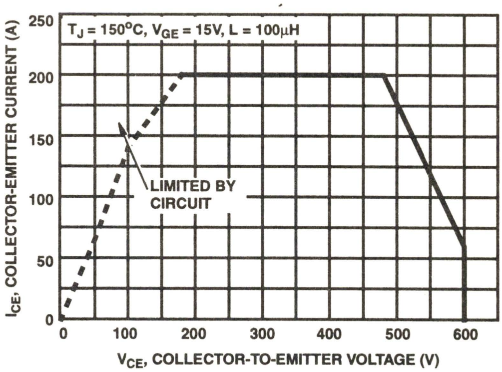


FIGURE 14. SWITCHING SAFE OPERATING AREA

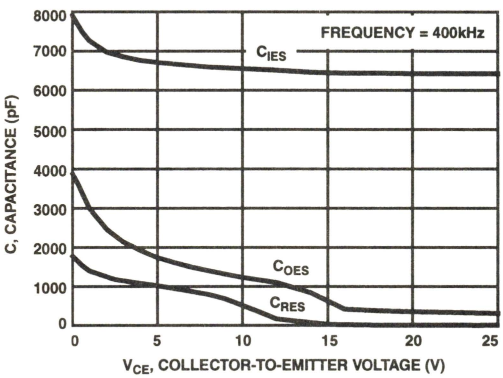


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

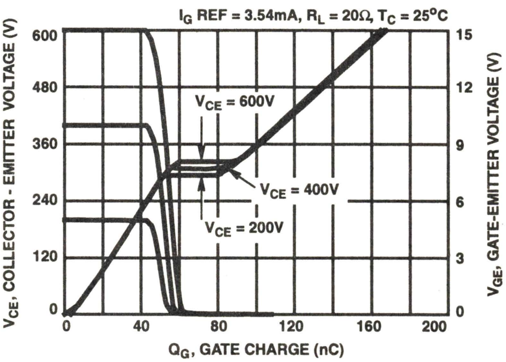


FIGURE 16. GATE CHARGE WAVEFORMS

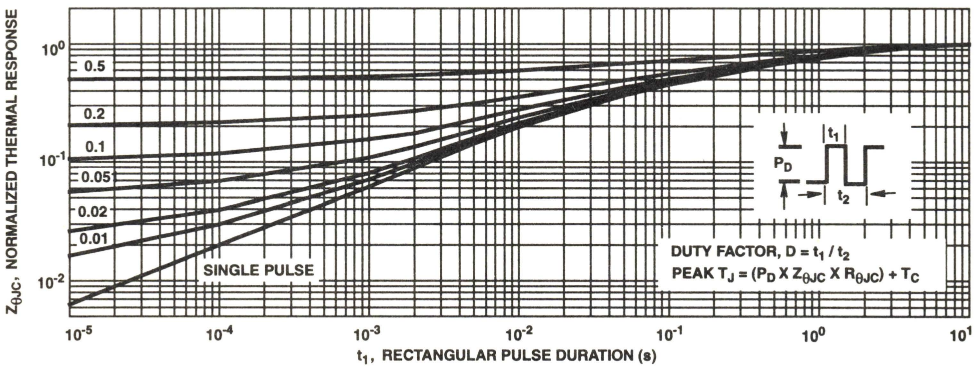


FIGURE 17. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

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Test Circuit and Waveform

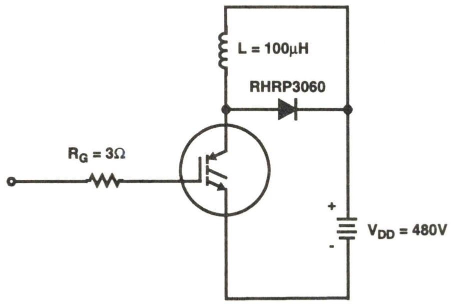
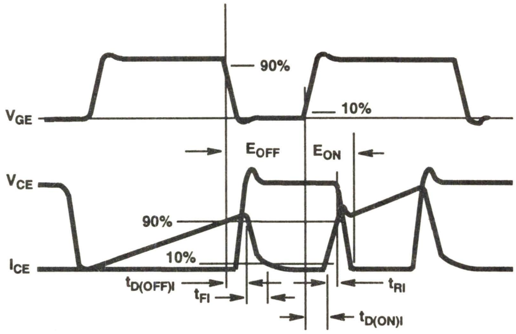


FIGURE 18. INDUCTIVE SWITCHING TEST CIRCUIT



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Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
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4. Devices should never be inserted into or removed from circuits with power on.
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6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
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f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 19.

Device turnoff delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 19. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

HARRIS SEMICONDUCTOR

HGTG30N60C3D

63A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diodes

January 1997

Features

- **63A, 600V at $T_C = 25^oC$**
- **Typical Fall Time .... 230ns at $T_J = 150^oC$**
- **Short Circuit Rating**
- **Low Conduction Loss**
- **Hyperfast Anti-Parallel Diode**

Description

The HGTG30N60C3D is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C. The IGBT used is the development type TA49051. The diode used in anti-parallel with the IGBT is the development type TA49053.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential.

PACKAGING AVAILABILITY

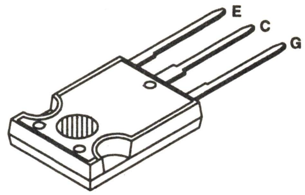
PART NUMBER	PACKAGE	BRAND
HGTG30N60C3D	TO-247	G30N60C3D

NOTE: When ordering, use the entire part number.

Formerly Developmental Type TA49014.

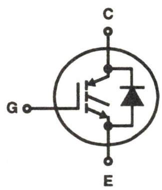
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTG30N60C3D	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	63	A
At $T_C = 110^oC$	I_{C110}	30	A
Average Diode Forward Current at 110°C	$I_{(AVG)}$	25	A
Collector Current Pulsed (Note 1)	I_{CM}	252	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$	SSOA	60A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	208	W
Power Dissipation Derating $T_C > 25^oC$		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	4	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	15	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = 125^oC$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4041.1**

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$, $V_{GE} = 0V$		15	25	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	μA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	3.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.5	1.8	V
			$T_C = 150^oC$	-	1.7	2.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.0	5.2	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA	SSOA	$T_J = 150^oC$, $V_{GE} = 15V$, $R_G = 3\Omega$, $L = 100\mu H$	$V_{CE(PK)} = 480V$	200	-	-	A
			$V_{CE(PK)} = 600V$	60	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8.1	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	162	180	nC
			$V_{GE} = 20V$	-	216	250	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 3\Omega$, $L = 100\mu H$		-	40	-	ns
Current Rise Time	t_{RI}			-	45	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	320	400	ns
Current Fall Time	t_{FI}			-	230	275	ns
Turn-On Energy	E_{ON}			-	1050	-	μJ
Turn-Off Energy (Note 3)	E_{OFF}			-	2500	-	μJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 30A$		-	1.75	2.2	V
Diode Reverse Recovery Time	t_{rr}	$I_{EC} = 30A$, $dI_{EC}/dt = 100A/\mu s$		-	52	60	ns
		$I_{EC} = 1.0A$, $dI_{EC}/dt = 100A/\mu s$		-	42	50	ns
Thermal Resistance	$R_{\theta JC}$	IGBT		-	-	0.6	$^oC/W$
		Diode		-	-	1.3	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTG30N60C3D was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

Typical Performance Curves

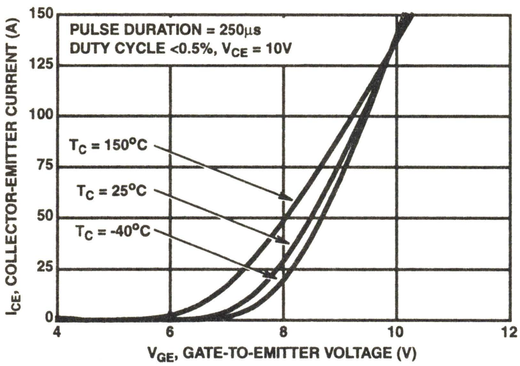


FIGURE 1. TRANSFER CHARACTERISTICS

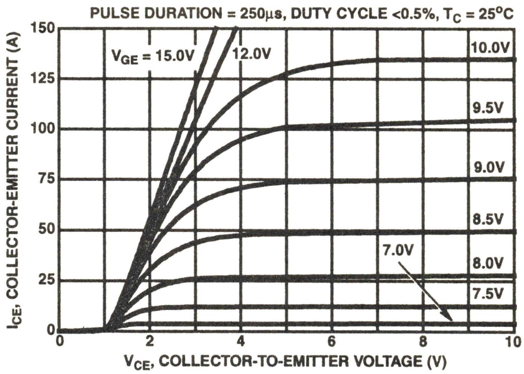


FIGURE 2. SATURATION CHARACTERISTICS

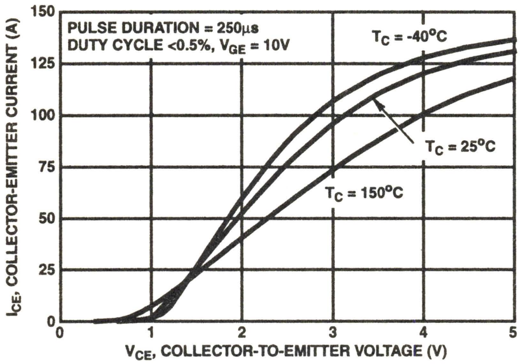


FIGURE 3. COLLECTOR-EMITTER ON-STATE VOLTAGE

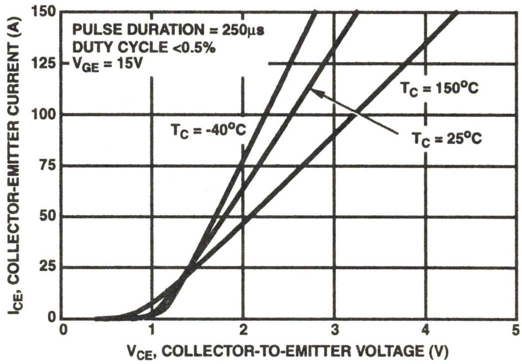


FIGURE 4. COLLECTOR-EMITTER ON-STATE VOLTAGE

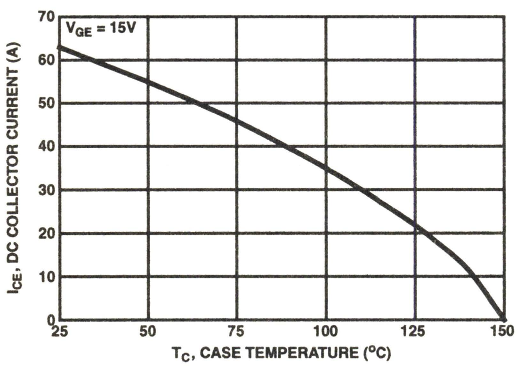


FIGURE 5. MAX. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

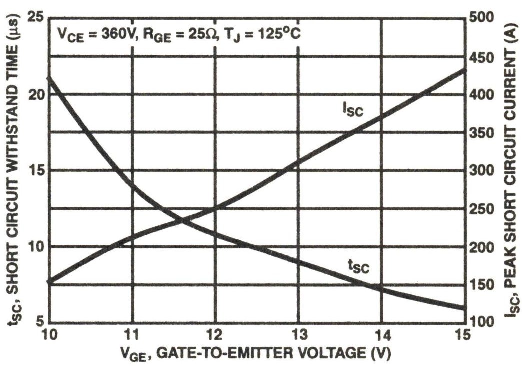


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

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Typical Performance Curves (Continued)

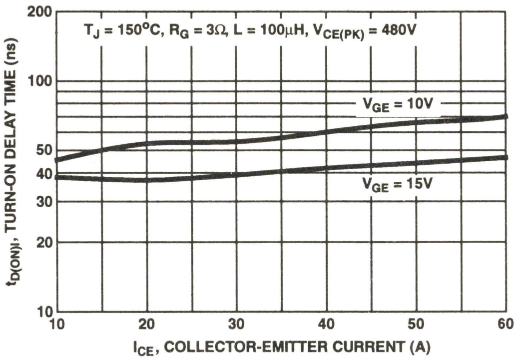


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

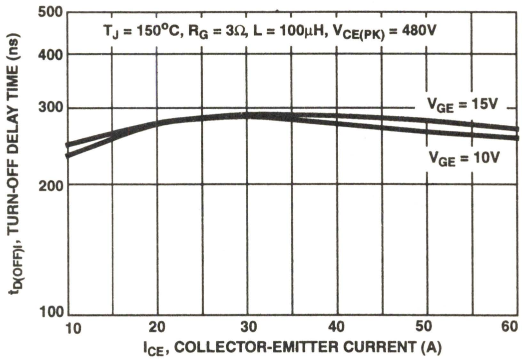


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

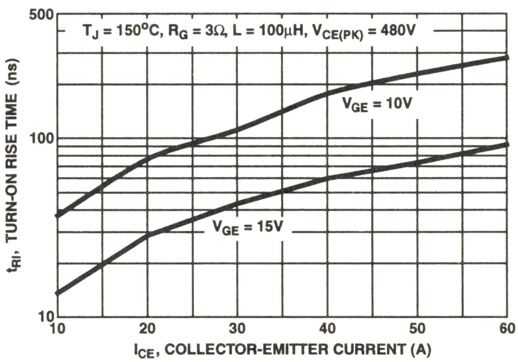


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

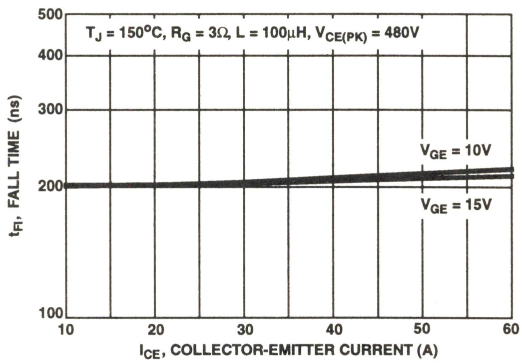


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

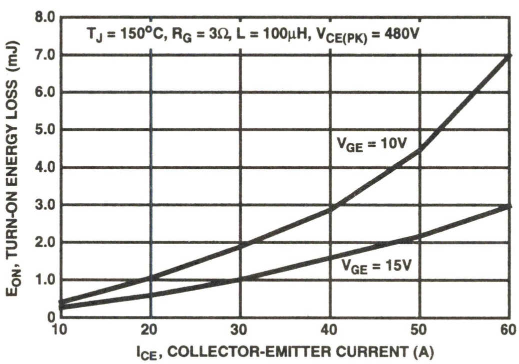
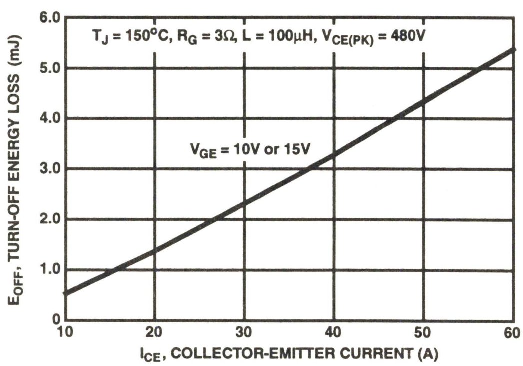


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT



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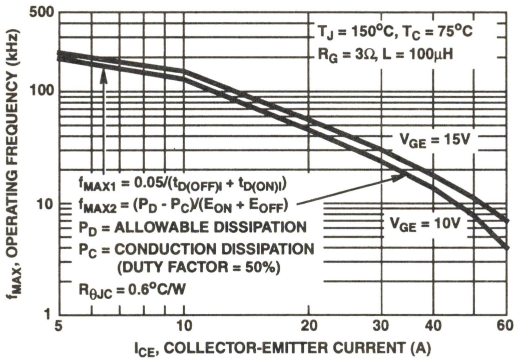
Typical Performance Curves (Continued)



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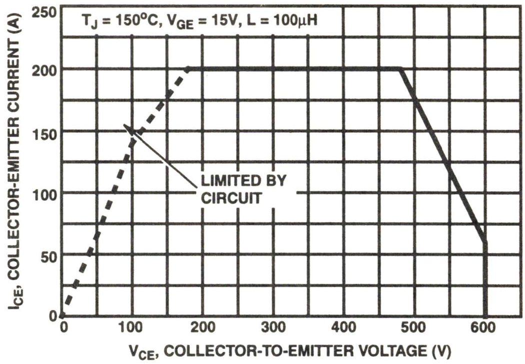

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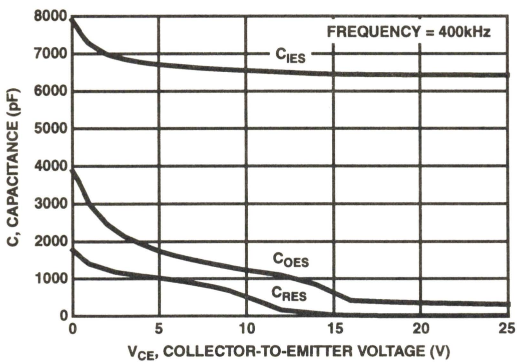

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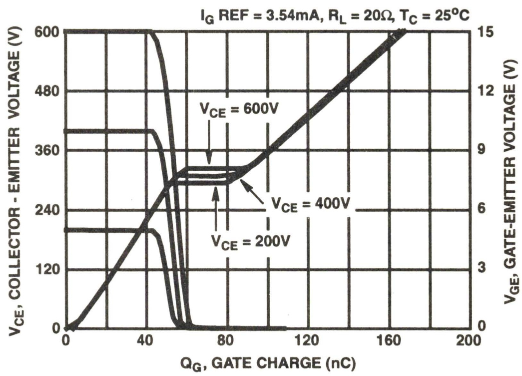

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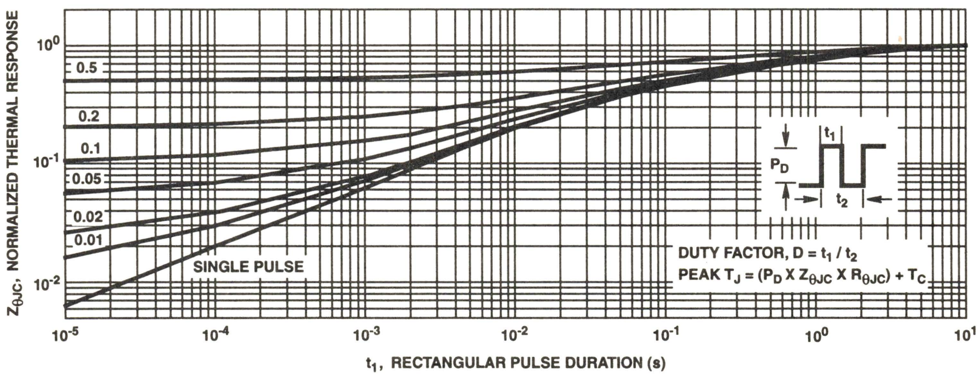

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Typical Performance Curves (Continued)

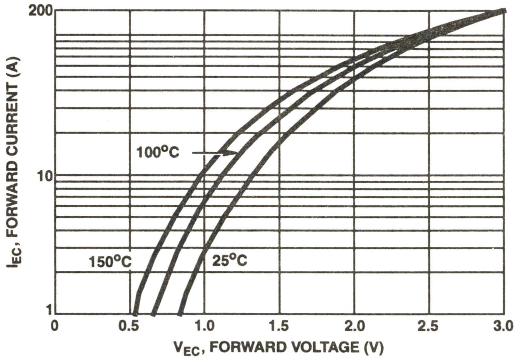


FIGURE 18. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

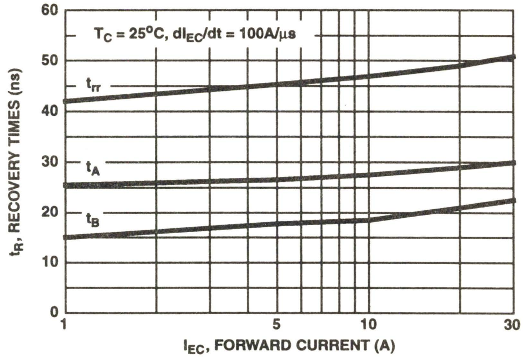
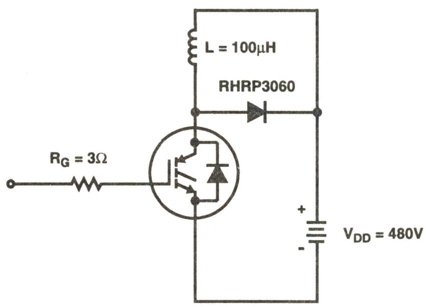


FIGURE 19. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveform



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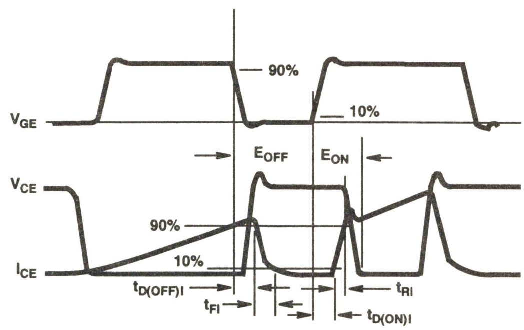

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3. Tips of soldering irons should be grounded.
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IGBT UFS SERIES SUPPLEMENT 4

B-SPEED UFS SERIES IGBTs

PAGE

B-Speed UFS Series IGBT Data Sheets

HGTP20N60B3, HGTG20N60B3	40A, 600V, UFS Series N-Channel IGBTs	4-3
HGTG20N60B3D	40A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode	4-9

HGTP20N60B3, HGTG20N60B3

HARRIS SEMICONDUCTOR

January 1997

40A, 600V, UFS Series N-Channel IGBTs

Features

- 40A, 600V at $T_C = 25^oC$
- 600V Switching SOA Capability
- Typical Fall Time .... 140ns at 150°C
- Short Circuit Rated
- Low Conduction Loss

Description

The HGTP20N60B3 and the HGTG20N60B3 are Generation 3 MOS gated high voltage switching devices combining the best features of MOSFETs and bipolar transistors. These devices have the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

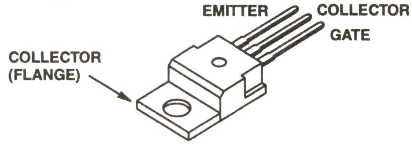
PART NUMBER	PACKAGE	BRAND
HGTP20N60B3	TO-220AB	G20N60B3
HGTG20N60B3	TO-247	G20N60B3

NOTE: When ordering, use the entire part number.

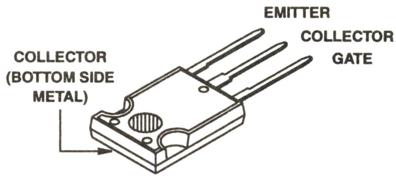
Formerly Developmental Type TA49050.

Package

JEDEC TO-220AB

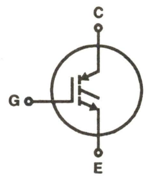


JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTP20N60B3 HGTG20N60B3	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage, $R_{GE} = 1M\Omega$	BV_{CGR}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	40	A
At $T_C = 110^oC$	I_{C110}	20	A
Collector Current Pulsed (Note 1)	I_{CM}	160	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_C = 150^oC$	SSOA	30A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	165	W
Power Dissipation Derating $T_C > 25^oC$		1.32	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	4	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	10	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_C = 125^oC$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3723.3**

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	μA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	1.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.8	2.0	V
			$T_C = 150^oC$	-	2.1	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.0	5.0	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA	SSOA	$T_C = 150^oC$, $V_{GE} = 15V$, $R_G = 10\Omega$, $L = 45\mu H$	$V_{CE(PK)} = 480V$	100	-	-	A
			$V_{CE(PK)} = 600V$	30	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	80	105	nC
			$V_{GE} = 20V$	-	105	135	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_C = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 10\Omega$, $L = 100\mu H$		-	25	-	ns
Current Rise Time	t_{RI}			-	20	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	220	275	ns
Current Fall Time	t_{FI}			-	140	200	ns
Turn-On Energy	E_{ON}			-	475	-	μJ
Turn-Off Energy (Note 3)	E_{OFF}			-	1050	-	μJ
Thermal Resistance	$R_{\theta JC}$			-	-	0.76	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$) The HGTP20N60B3 and HGTG20N60B3 were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-on losses include diode losses.

Typical Performance Curves

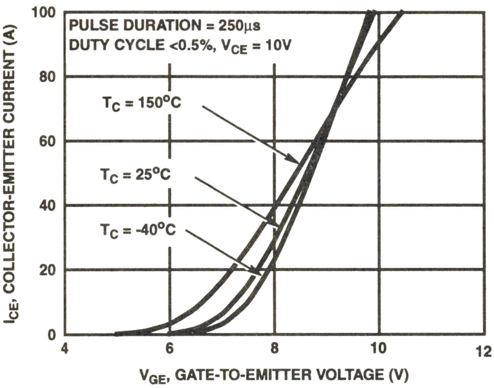


FIGURE 1. TRANSFER CHARACTERISTICS

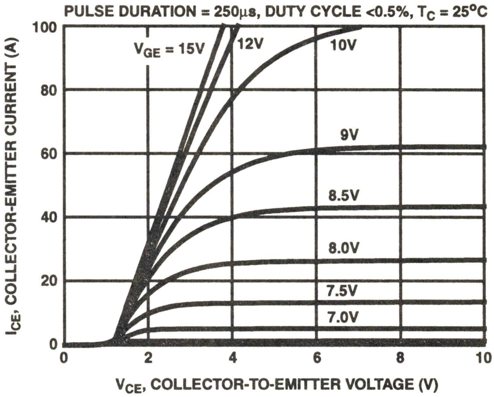


FIGURE 2. SATURATION CHARACTERISTICS

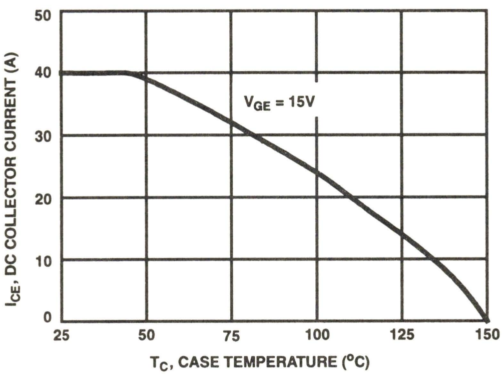


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

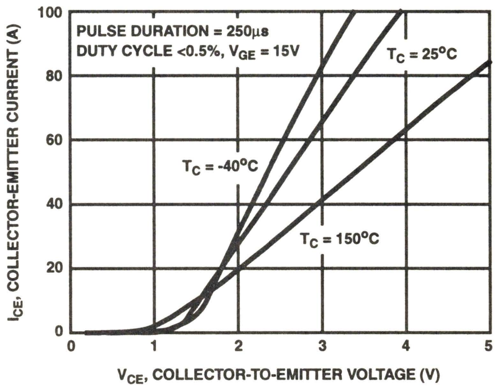


FIGURE 4. COLLECTOR-EMITTER ON - STATE VOLTAGE

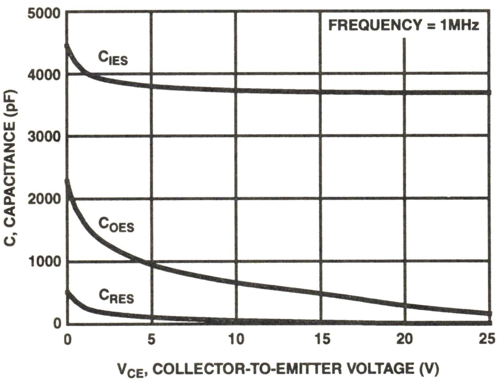


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

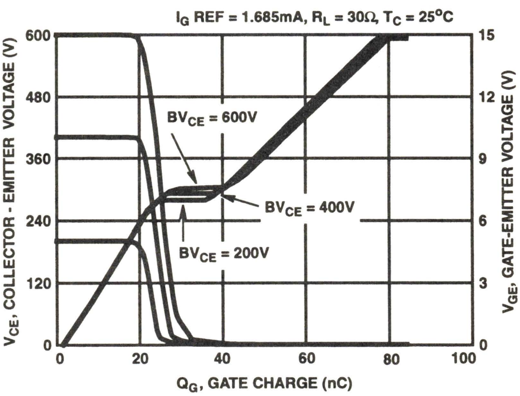


FIGURE 6. GATE CHARGE WAVEFORMS

B-SPEED UFS SERIES 4

Typical Performance Curves (Continued)

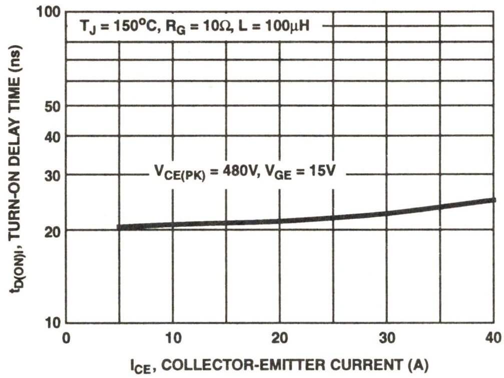


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

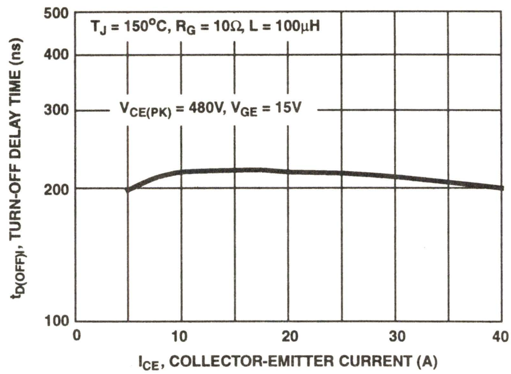


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

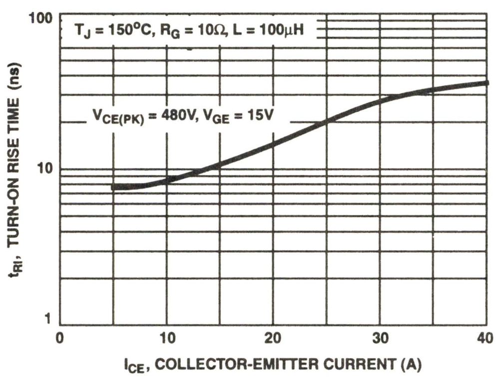


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

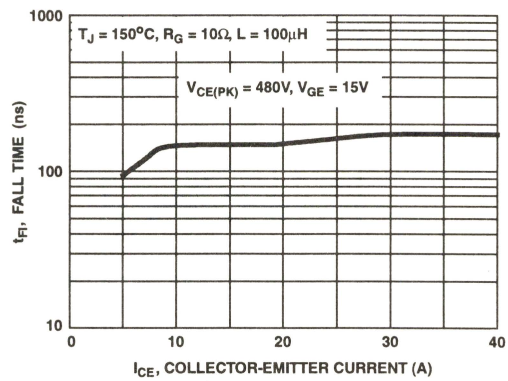


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

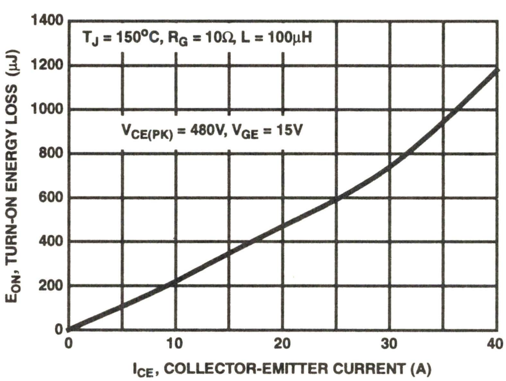


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

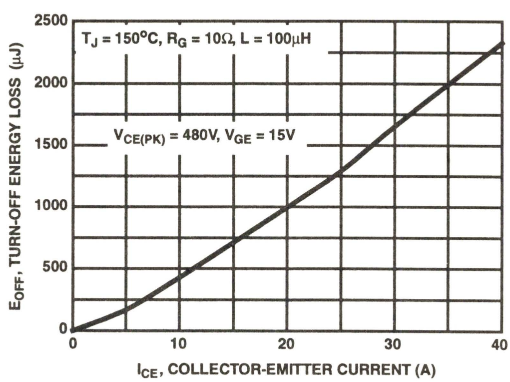


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

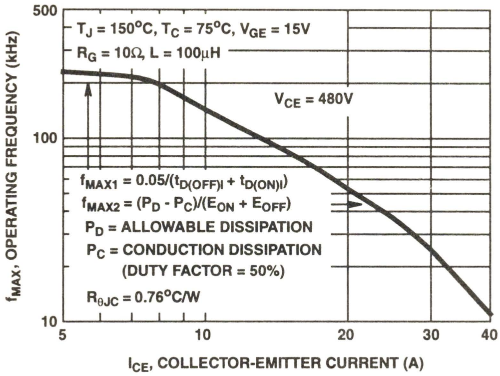


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

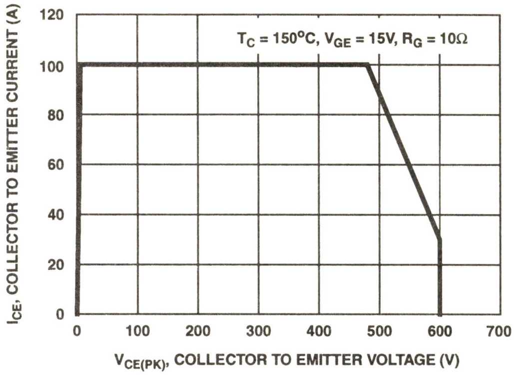


FIGURE 14. SWITCHING SAFE OPERATING AREA

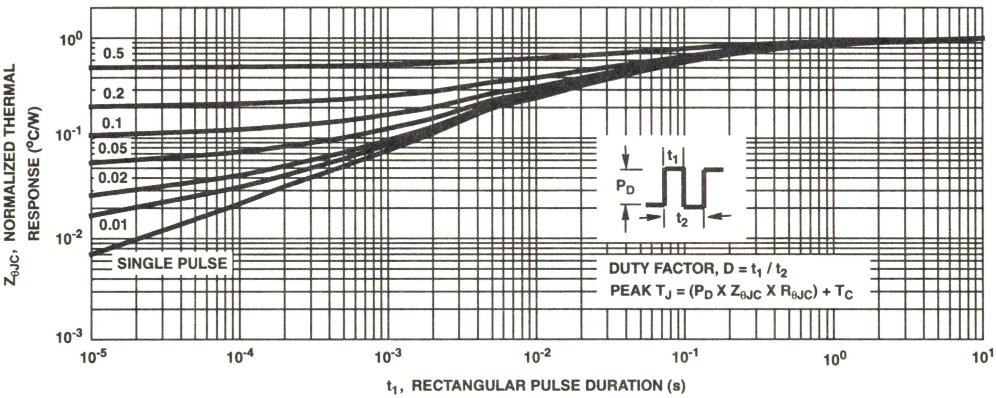


FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 17.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$.

The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 17. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

Test Circuit and Waveform

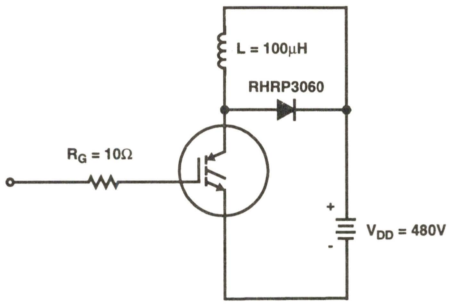


FIGURE 16. INDUCTIVE SWITCHING TEST CIRCUIT

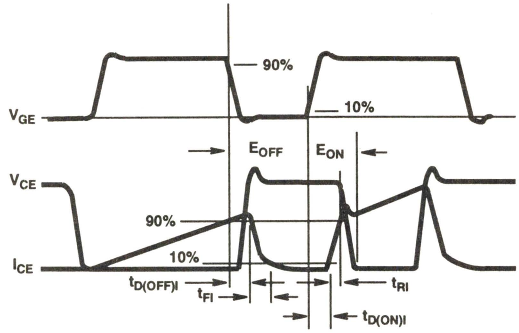


FIGURE 17. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBT's are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

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HGTG20N60B3D

40A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode

January 1997

Features

- **40A, 600V at $T_C = 25^oC$**
- **Typical Fall Time . . . . 140ns at 150°C**
- **Short Circuit Rated**
- **Low Conduction Loss**
- **Hyperfast Anti-Parallel Diode**

Description

The HGTG20N60B3D is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C. The diode used in anti-parallel with the IGBT is the RHRP3060.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential.

PACKAGING AVAILABILITY

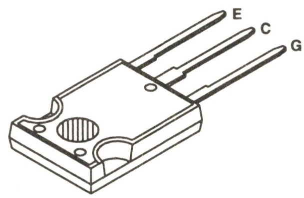
PART NUMBER	PACKAGE	BRAND
HGTG20N60B3D	TO-247	G20N60B3D

NOTE: When ordering, use the entire part number.

Formerly Developmental Type TA49016.

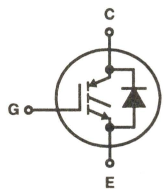
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTG20N60B3D	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage, $R_{GE} = 1M\Omega$	BV_{CGR}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	40	A
At $T_C = 110^oC$	I_{C110}	20	A
Average Diode Forward Current at 110°C	$I_{(AVG)}$	20	A
Collector Current Pulsed (Note 1)	I_{CM}	160	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_C = 150^oC$	SSOA	80A at 0.8 BV_{CES}	
Power Dissipation Total at $T_C = 25^oC$	P_D	165	W
Power Dissipation Derating $T_C > 25^oC$		1.32	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	4	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	10	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_C = 125^oC$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
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4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3739.4**

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	2.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.8	2.0	V
			$T_C = 150^oC$	-	2.1	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.0	5.0	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA	SSOA	$T_C = 150^oC$ $V_{GE} = 15V$, $R_G = 10\Omega$, $L = 45\mu H$	$V_{CE(PK)} = 480V$	100	-	-	A
			$V_{CE(PK)} = 600V$	30	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	80	105	nC
			$V_{GE} = 20V$	-	105	135	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_C = 150^oC$, $I_{CE} = I_{C110}$ $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$ $R_G = 10\Omega$, $L = 100\mu H$		-	25	-	ns
Current Rise Time	t_{RI}			-	20	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	220	275	ns
Current Fall Time	t_{FI}			-	140	200	ns
Turn-On Energy	E_{ON}			-	475	-	µJ
Turn-Off Energy (Note 3)	E_{OFF}			-	1050	-	µJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 20A$		-	1.5	1.9	V
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 20A$, $dI_{EC}/dt = 100A/\mu s$		-	-	55	ns
		$I_{EC} = 1A$, $dI_{EC}/dt = 100A/\mu s$		-	-	45	ns
Thermal Resistance	$R_{\theta JC}$	IGBT		-	-	0.76	$^oC/W$
		Diode		-	-	1.2	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$) The HGTG20N60B3D was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

Typical Performance Curves

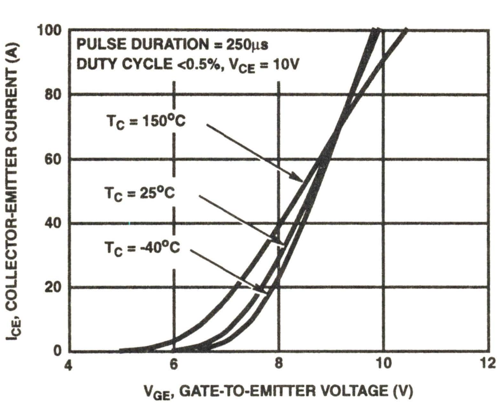

FIGURE 1. TRANSFER CHARACTERISTICS

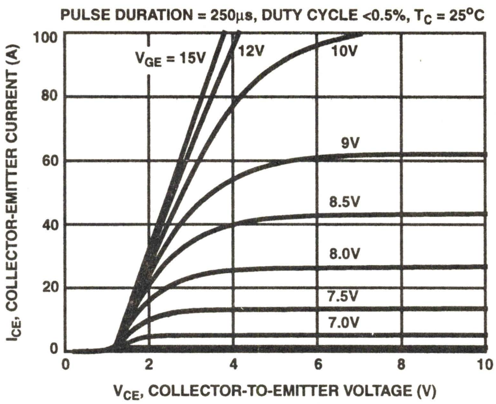

FIGURE 2. SATURATION CHARACTERISTICS

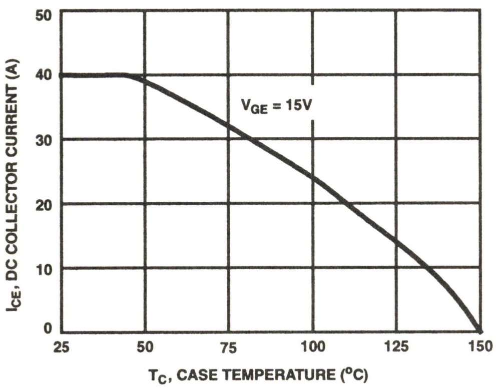

FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

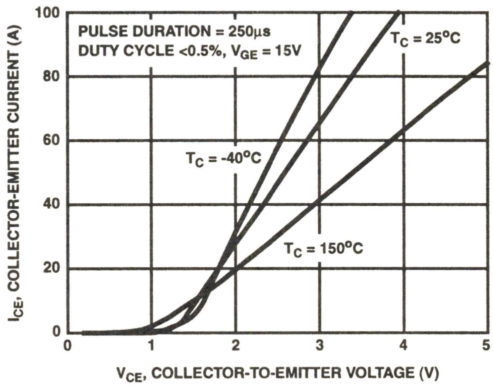

FIGURE 4. COLLECTOR-EMITTER ON-STATE VOLTAGE

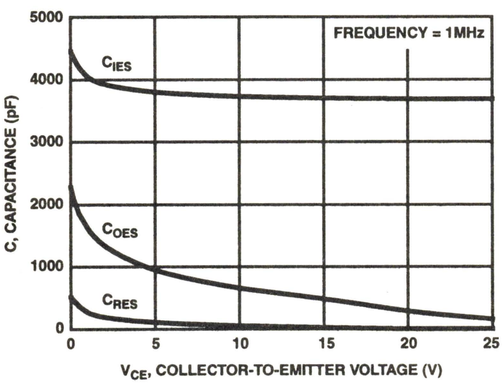

FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

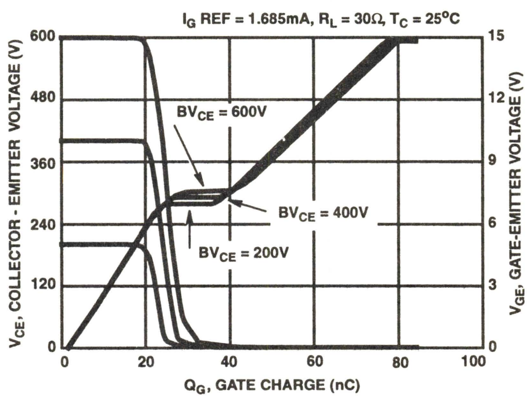

FIGURE 6. GATE CHARGE WAVEFORMS

Typical Performance Curves (Continued)

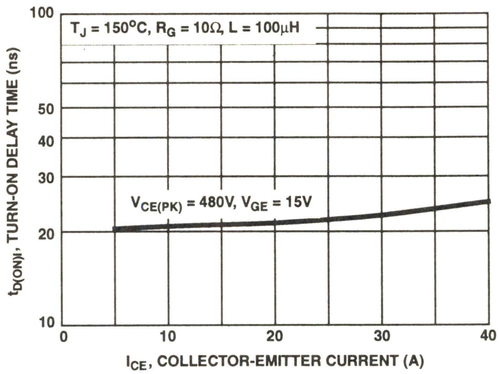

FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

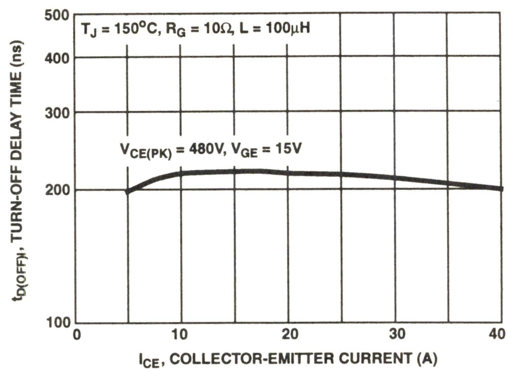

FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

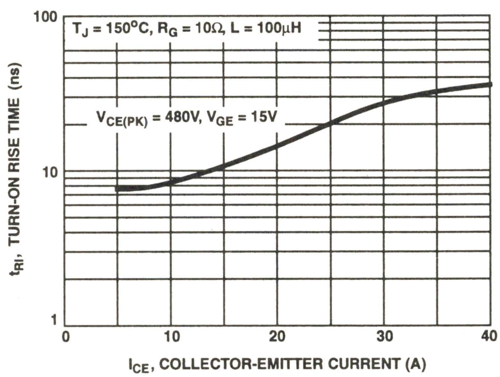

FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

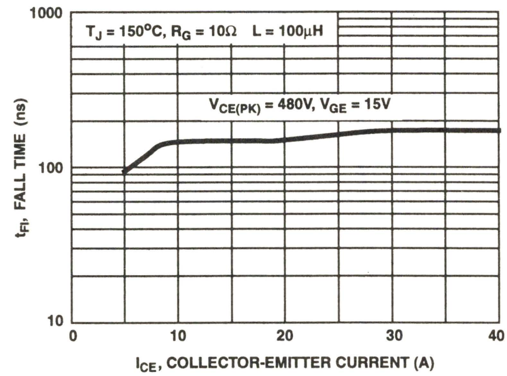

FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

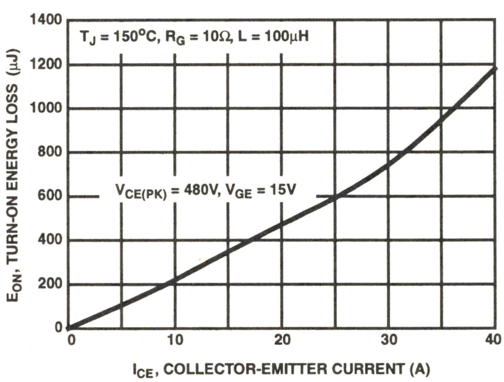

FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

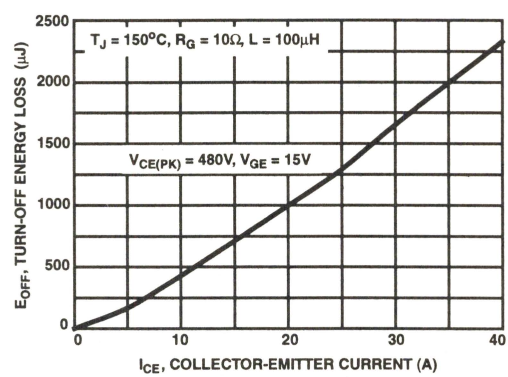

FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

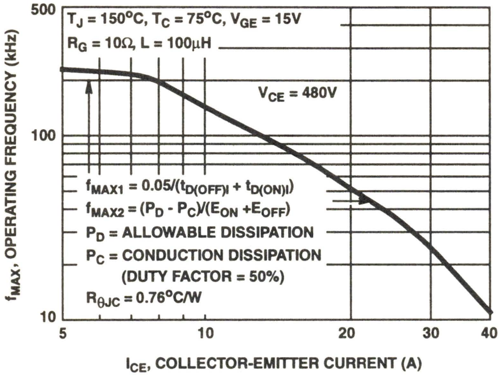

FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

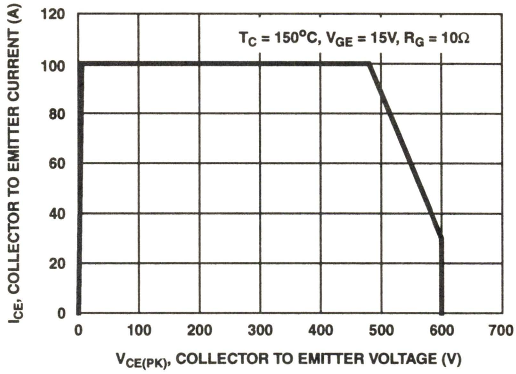

FIGURE 14. SWITCHING SAFE OPERATING AREA

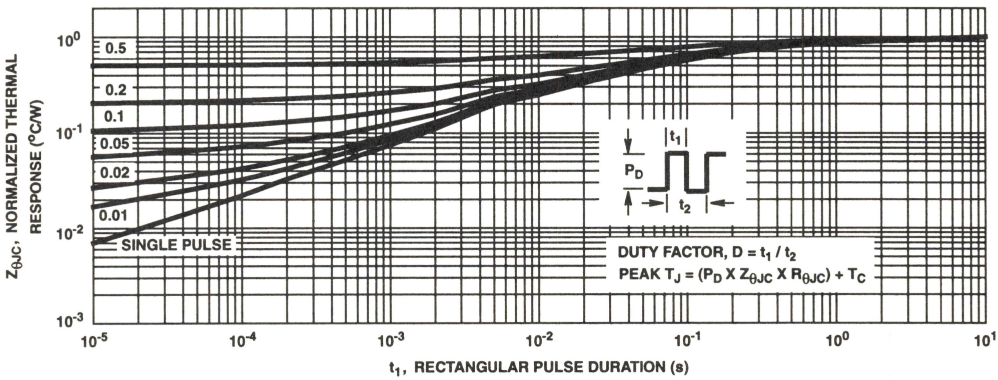

FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

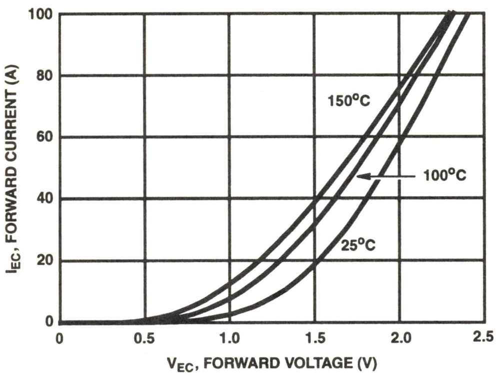

FIGURE 16. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

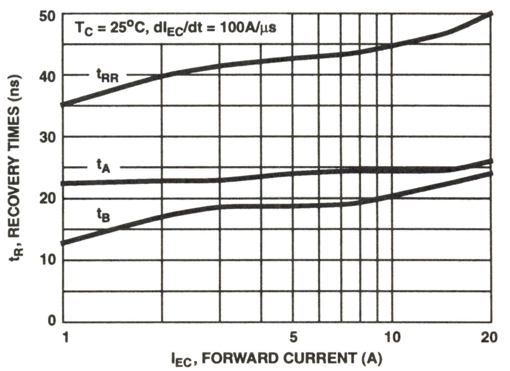

FIGURE 17. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveform

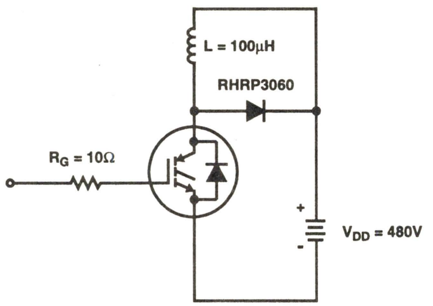

FIGURE 18. INDUCTIVE SWITCHING TEST CIRCUIT

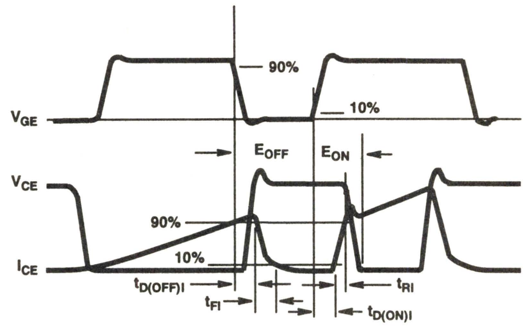

FIGURE 19. SWITCHING TEST WAVEFORMS

Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I}\ t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 19.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 19. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and discharge procedures, however, IGBT's are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

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IGBT UFS SERIES SUPPLEMENT 5

RUGGED UFS SERIES IGBTs

		PAGE
Rugged UFS Series IGBT Data Sheets		
HGTG20N60C3R, HGTP20N60C3R, HGT1S20N60C3R, HGT1S20N60C3RS	40A, 600V, Rugged UFS Series N-Channel IGBTs	5-3
HGTG20N60C3DR	40A, 600V, Rugged, UFS Series N-Channel IGBT with Anti-Parallel Ultrafast Diode	5-9
HGTG27N60C3R	54A, 600V, Rugged UFS Series N-Channel IGBT	5-16
HGTG27N60C3DR	54A, 600V, Rugged UFS Series N-Channel IGBT with Anti-Parallel Ultrafast Diode	5-22

5

RUGGED UFS SERIES

HGTG20N60C3R, HGTP20N60C3R, HGT1S20N60C3R, HGT1S20N60C3RS

HARRIS SEMICONDUCTOR

January 1997

40A, 600V, Rugged UFS Series N-Channel IGBTs

Features

- 40A, 600V $T_J = 25^oC$
- 600V Switching SOA Capability
- Typical Fall Time at $T_J = 150^oC$ 330ns
- Short Circuit Rating at $T_J = 150^oC$............. 10µs
- Low Conduction Loss

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTP20N60C3R	TO-220AB	20N60C3R
HGTG20N60C3R	TO-247	20N60C3R
HGT1S20N60C3R	TO-262AA	20N60C3R
HGT1S20N60C3RS	TO-263AB	20N60C3R

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in the tape and reel, i.e., HGT1S20N60C3RS9A.

Description

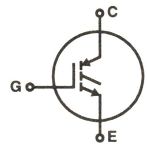
This family of IGBTs was designed for optimum performance in the demanding world of motor control operation as well as other high voltage switching applications. These devices demonstrate RUGGED performance capability when subjected to harsh SHORT CIRCUIT WITHSTAND TIME (SCWT) conditions. The parts have ULTRAFAST (UFS) switching speed while the on-state conduction losses have been kept at a low level.

The electrical specifications include typical Turn-On and Turn-Off dv/dt ratings. These ratings and the Turn-On ratings include the effect of the diode in the test circuit (Figure 16). The data was obtained with the diode at the same T_J as the IGBT under test.

Formerly Developmental Type TA49047.

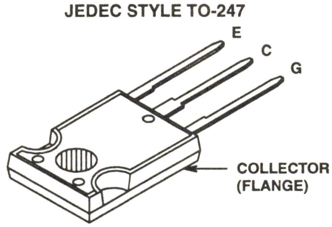
Terminal Diagram

N-CHANNEL ENHANCEMENT MODE

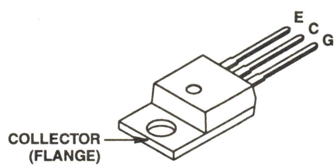


Packaging

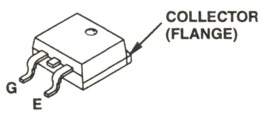
JEDEC STYLE TO-247



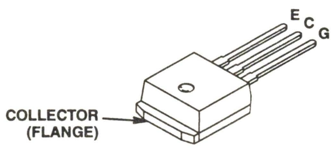
JEDEC TO-220AB (ALTERNATE VERSION)



JEDEC TO-263AB



JEDEC TO-262AA



HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number 4226.1

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		ALL TYPES	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	40	A
At $T_C = 110^oC$	I_{C110}	20	A
Collector Current Pulsed (Note 1)	I_{CM}	80	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Fig. 12	SSOA	80A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	164	W
Power Dissipation Derating $T_C > 25^oC$		1.32	W/°C
Reverse Voltage Avalanche Energy	E_{ARV}	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	10	µs

NOTES:

1. Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 440V$, $T_J = 150^oC$, $R_{GE} = 10\Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$, $V_{GE} = 0V$		15	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	3.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.8	2.2	V
			$T_C = 150^oC$	-	2.1	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	3.5	6.3	7.5	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA (See Figure 12)	SSOA	$T_J = 150^oC$, $R_G = 10\Omega$, $V_{GE} = 15V$	$V_{CE(PK)} = 600V$, $L = 1mH$	80	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	9.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{ES}$	$V_{GE} = 15V$	-	87	110	nC
			$V_{GE} = 20V$	-	116	150	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 10\Omega$, $L = 1mH$; Diode used in test circuit RURP1560 at 150°C		-	34	-	ns
Current Rise Time	t_{RI}			-	40	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	390	500	ns
Current Fall Time	t_{FI}			-	330	400	ns
Turn-Off Voltage dv/dt (Note 3)	dV_{CE}/dt			-	1.3	-	V/ns
Turn-On Voltage dv/dt (Note 3)	dV_{CE}/dt			-	7.0	-	V/ns
Turn-On Energy (Note 4)	E_{ON}			-	2.3	-	mJ
Turn-Off Energy (Note 5)	E_{OFF}			-	3.0	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	-	0.76	°C/W

NOTES:

3. dV_{CE}/dt depends on the diode used and the temperature of the diode.
4. Turn-On Energy Loss (E_{ON}) includes diode losses and is defined as the integral of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the collector voltage equals $V_{CE(ON)}$. This value of E_{ON} was obtained with a RURP1560 diode at $T_J = 150^oC$. A different diode or temperature will result in a different E_{ON}. For example with diode at $T_J = 25^oC$ E_{ON} is about one half the value at 150°C.
5. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

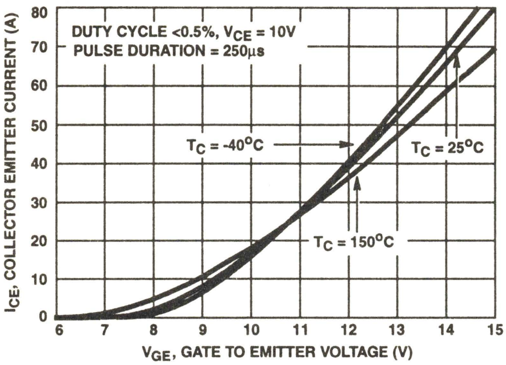


FIGURE 1. TRANSFER CHARACTERISTICS

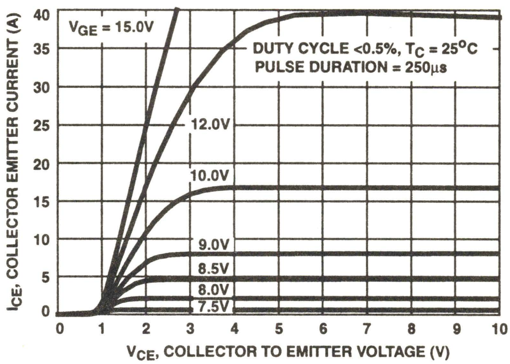


FIGURE 2. SATURATION CHARACTERISTICS

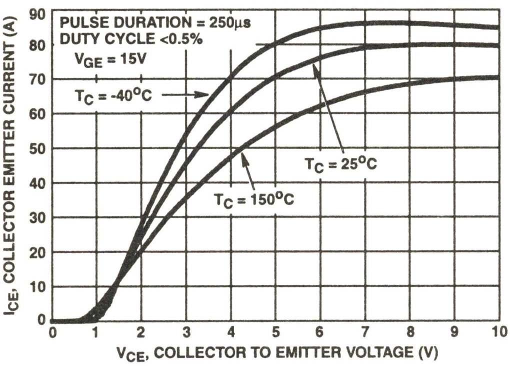


FIGURE 3. COLLECTOR EMITTER ON STATE VOLTAGE

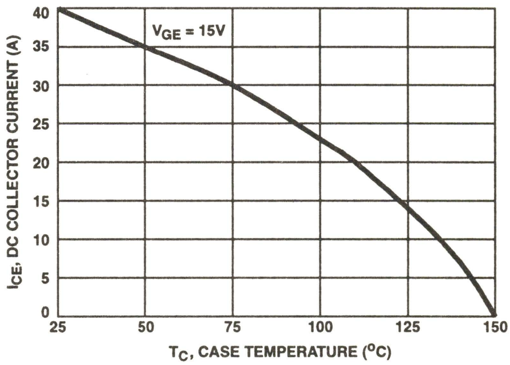


FIGURE 4. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

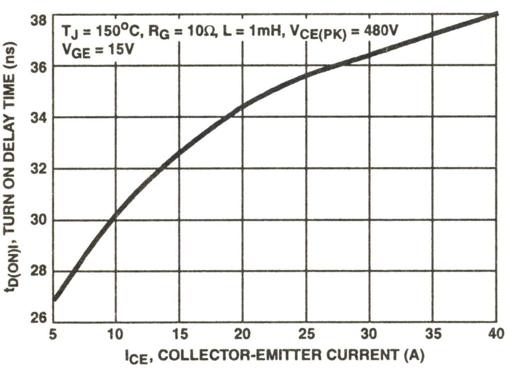


FIGURE 5. TURN ON DELAY TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

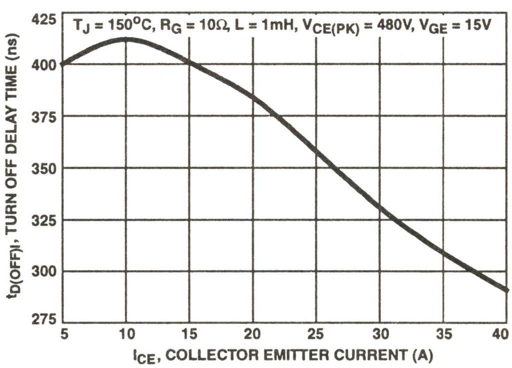


FIGURE 6. TURN OFF DELAY TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

Typical Performance Curves (Continued)

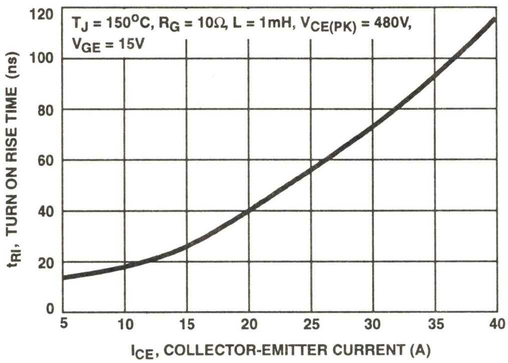


FIGURE 7. TURN ON RISE TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

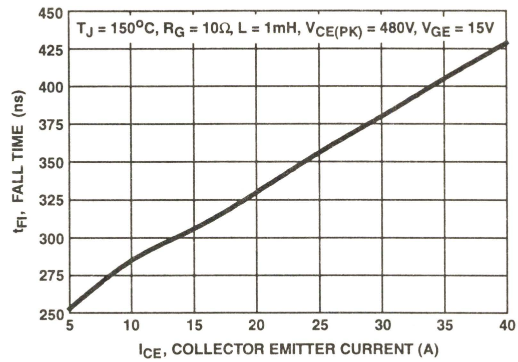


FIGURE 8. TURN OFF FALL TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

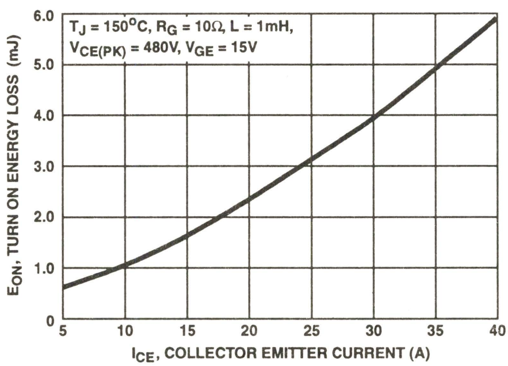


FIGURE 9. TURN ON ENERGY LOSS AS A FUNCTION OF COLLECTOR EMITTER CURRENT

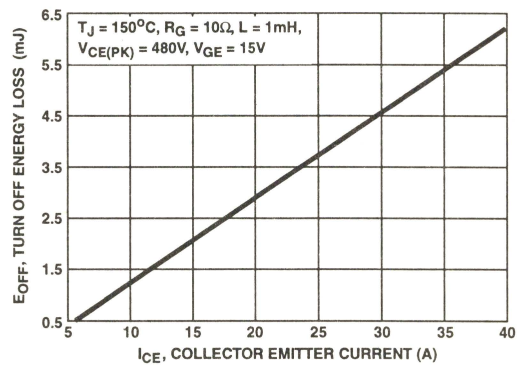


FIGURE 10. TURN OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR EMITTER CURRENT

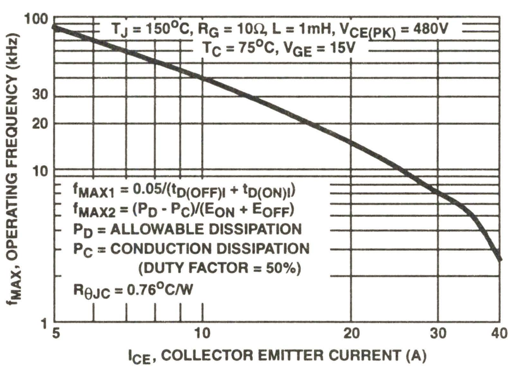


FIGURE 11. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR EMITTER CURRENT

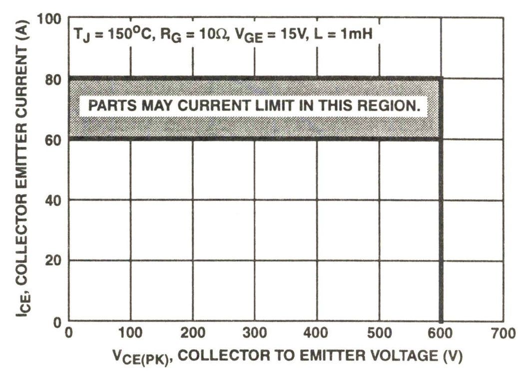


FIGURE 12. SWITCHING SAFE OPERATING AREA

Typical Performance Curves (Continued)

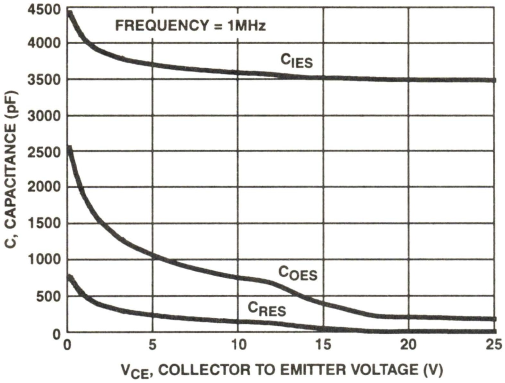


FIGURE 13. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

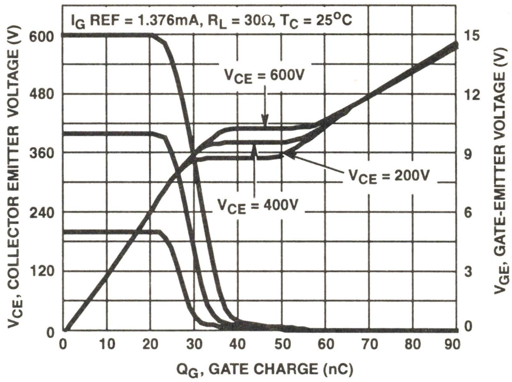


FIGURE 14. GATE CHARGE WAVEFORMS

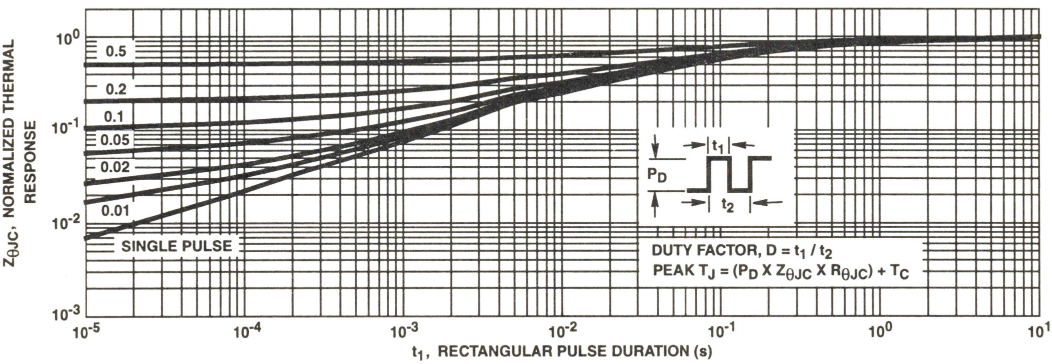


FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Test Circuit and Waveform

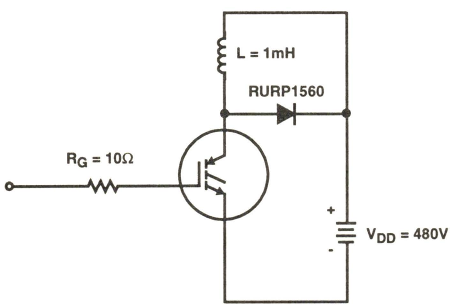


FIGURE 16. INDUCTIVE SWITCHING TEST CIRCUIT

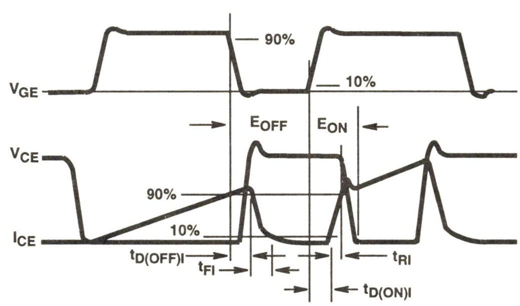


FIGURE 17. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 11) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (ICE) plots are possible using the information shown for a typical unit in Figures 3, 5, 6, 9 and 10. The operating frequency plot (Figure 11) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Dead-time (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 17. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 11) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 17. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

HGTG20N60C3DR

40A, 600V, Rugged, UFS Series N-Channel IGBT with Anti-Parallel Ultrafast Diode

January 1997

Features

- 40A, 600V at $T_C = 25^oC$
- 600V Switching SOA Capability
- Typical Fall Time at $T_J = 150^oC$ 330ns
- Short Circuit Rating at $T_J = 150^oC$ 10μs
- Low Conduction Loss
- Ultrafast Anti-Parallel Diode

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTG20N60C3DR	TO-247	20N60C3DR

NOTE: When ordering, use the entire part number.

Description

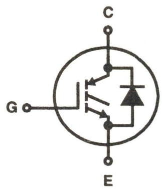
This family of IGBTs was designed for optimum performance in the demanding world of motor control operation as well as other high voltage switching applications. These devices demonstrate RUGGED performance capability when subjected to harsh SHORT CIRCUIT WITHSTAND TIME (SCWT) conditions. The parts have ULTRAFAST (UFS) switching speed while the on-state conduction losses have been kept at a low level.

The electrical specifications include typical Turn-On and Turn-Off dv/dt ratings. These ratings and the Turn-On ratings include the effect of the diode in the test circuit (Figure 18). The data was obtained with the diode at the same T_J as the IGBT under test. The diode used in anti-parallel with the IGBT is the RURP1560. The IGBT is development type TA49047.

Formerly development type TA49017.

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE

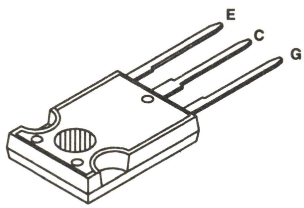


5

RUGGED UFS SERIES

Packaging

JEDEC STYLE TO-247



HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

	Symbol	HGTG20N60C3DR	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	40	A
At $T_C = 110^oC$	I_{C110}	20	A
Average Diode Forward Current	$I_{EC(AVG)}$	15	A
Collector Current Pulsed (Note 1)	I_{CM}	80	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_C = 150^oC$	SSOA	80A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	164	W
Power Dissipation Derating $T_C > 25^oC$		1.32	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	10	µs

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 440V$, $T_J = 150^oC$, $R_{GE} = 10\Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
			$T_C = 150^oC$	-	-	3.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.8	2.2	V
			$T_C = 150^oC$	-	2.1	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$		3.5	6.3	7.5	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA (See Figure 12)	SSOA	$T_J = 150^oC$, $R_G = 10\Omega$, $V_{GE} = 15V$, $V_{CE(PK)} = 600V$, L = 1mH		80	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	9.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{ES}$	$V_{GE} = 15V$	-	87	110	nC
			$V_{GE} = 20V$	-	116	150	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$ $I_{CE} = I_{C110}$ $V_{CE(PK)} = 0.8\ BV_{CES}$ $V_{GE} = 15V$ $R_G = 10\Omega$ L = 1mH Diode used in test circuit RURP1560 at 150^{o}C		-	34	-	ns
Current Rise Time	t_{RI}			-	40	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	390	500	ns
Current Fall Time	t_{FI}			-	330	400	ns
Turn-Off Voltage dv/dt (Note 3)	dV_{CE}/dt			-	1.3	-	V/ns
Turn-On Voltage dv/dt (Note 3)	dV_{CE}/dt			-	7.0	-	V/ns
Turn-On Energy (Note 4)	E_{ON}			-	2.3	-	mJ
Turn-Off Energy (Note 5)	E_{OFF}			-	3.0	-	mJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 20A$		-	-	1.6	V

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Diode Reverse Recovery Time	t_{rr}	I_{EC} = 1A, dI_{EC}/dt = 200A/µs	-	-	45	ns
		I_{EC} = 20A, dI_{EC}/dt = 200A/µs	-	-	58	ns
Thermal Resistance	$R_{\theta JC}$	IGBT	-	-	0.76	$^oC/W$
		Diode	-	-	1.5	$^oC/W$

NOTES:

3. dV_{CE}/dt depends on the diode used and the temperature of the diode.
4. Turn-On Energy Loss (E_{ON}) includes losses due to the diode recovery and is defined as the integral of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the collector voltage equals V_{CE}(ON). This value of E_{ON} was obtained with a RURP1560 diode at T_J = 150°C. A different diode or temperature will result in a different E_{ON}. For example with diode at T_J = 25°C, E_{ON} is about one half the value of E_{ON} with diode at T_J =150°C.
5. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A). All devices were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

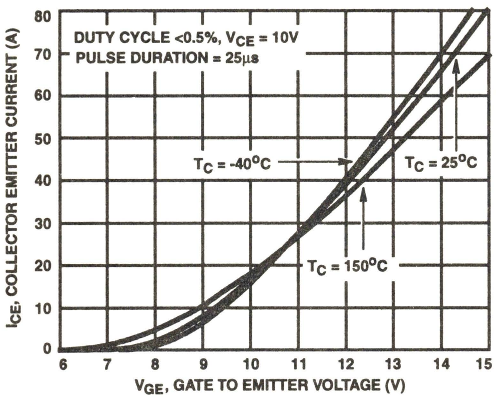


FIGURE 1. TRANSFER CHARACTERISTICS

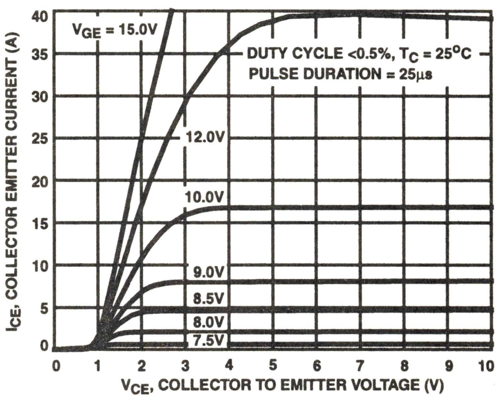


FIGURE 2. SATURATION CHARACTERISTICS

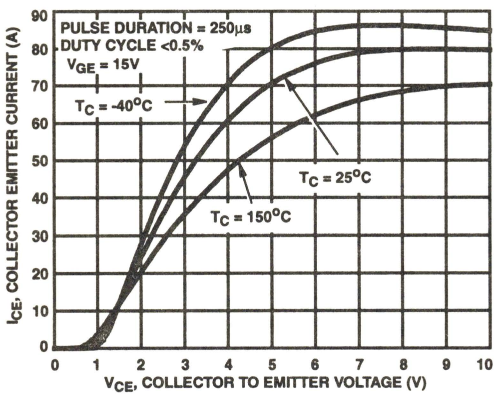


FIGURE 3. COLLECTOR EMITTER ON STATE VOLTAGE

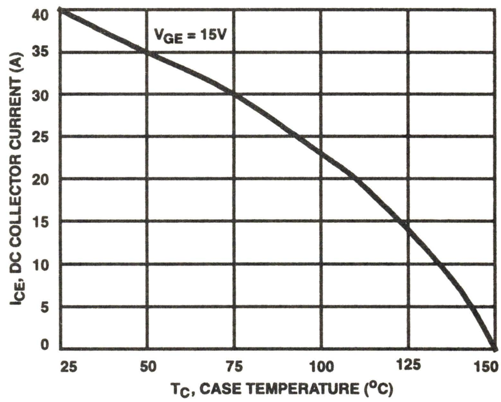


FIGURE 4. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

Typical Performance Curves (Continued)

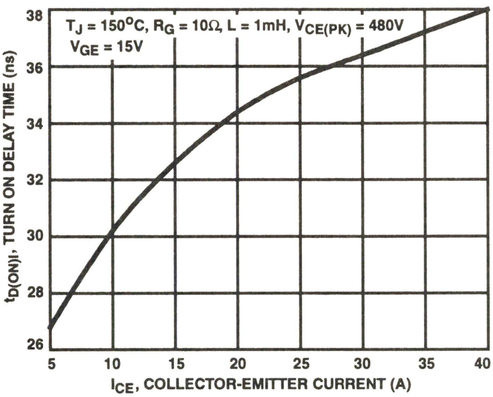


FIGURE 5. TURN ON DELAY TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

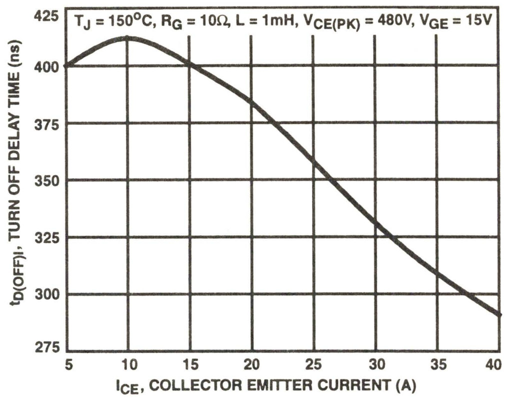


FIGURE 6. TURN OFF DELAY TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

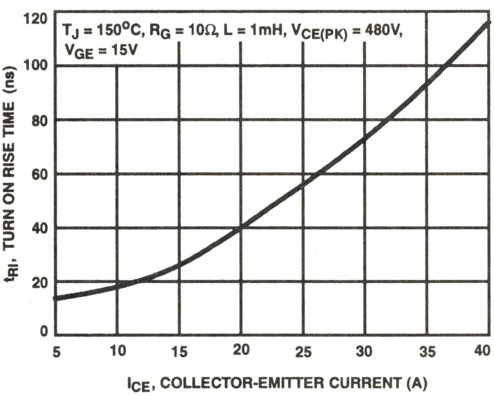


FIGURE 7. TURN ON RISE TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

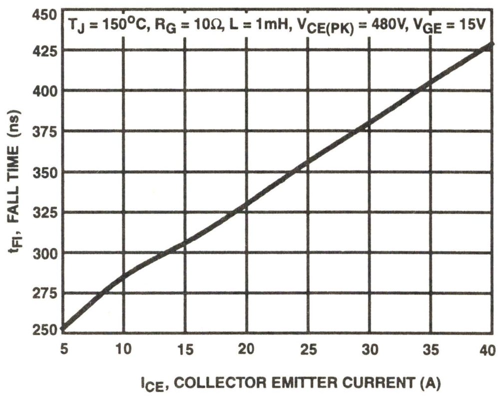


FIGURE 8. TURN OFF FALL TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

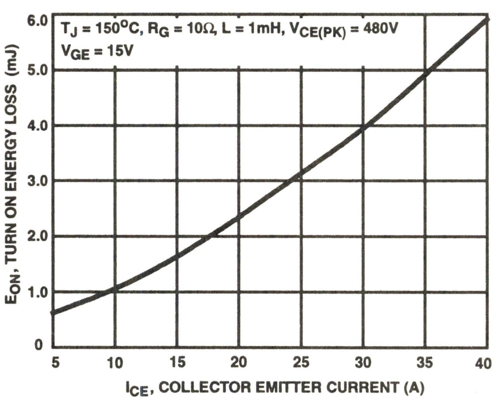


FIGURE 9. TURN ON ENERGY LOSS AS A FUNCTION OF COLLECTOR EMITTER CURRENT

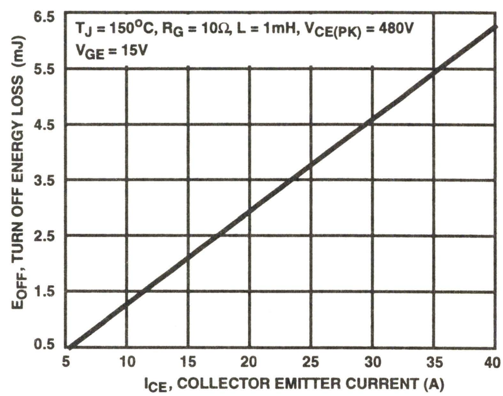


FIGURE 10. TURN OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR EMITTER CURRENT

Typical Performance Curves (Continued)

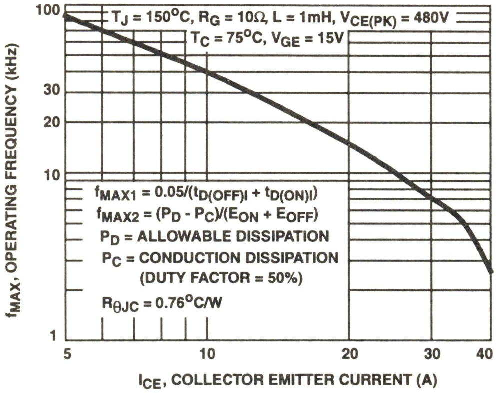


FIGURE 11. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR EMITTER CURRENT

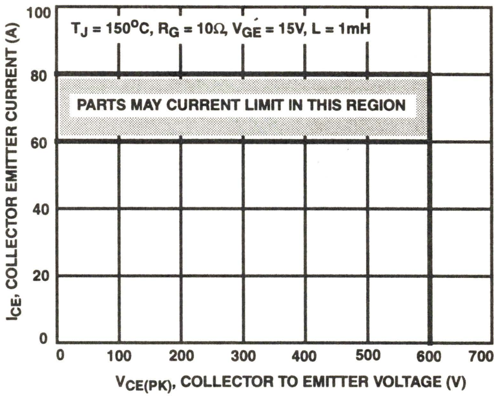


FIGURE 12. SWITCHING SAFE OPERATING AREA

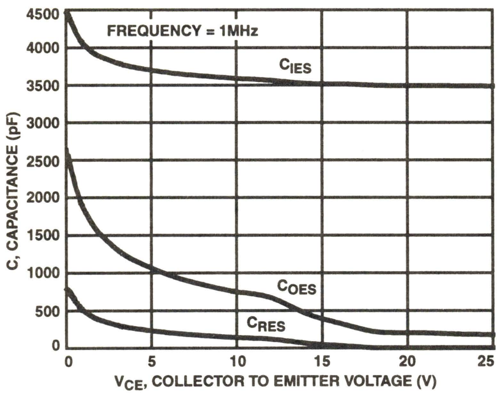


FIGURE 13. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

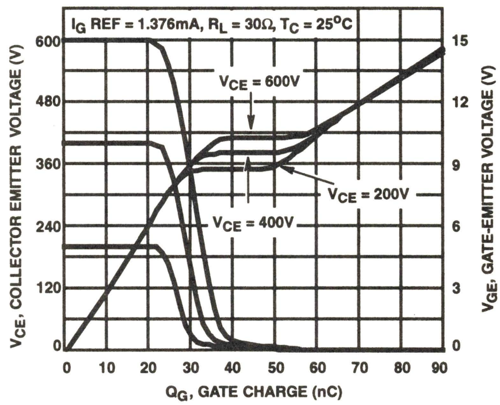


FIGURE 14. GATE CHARGE WAVEFORMS

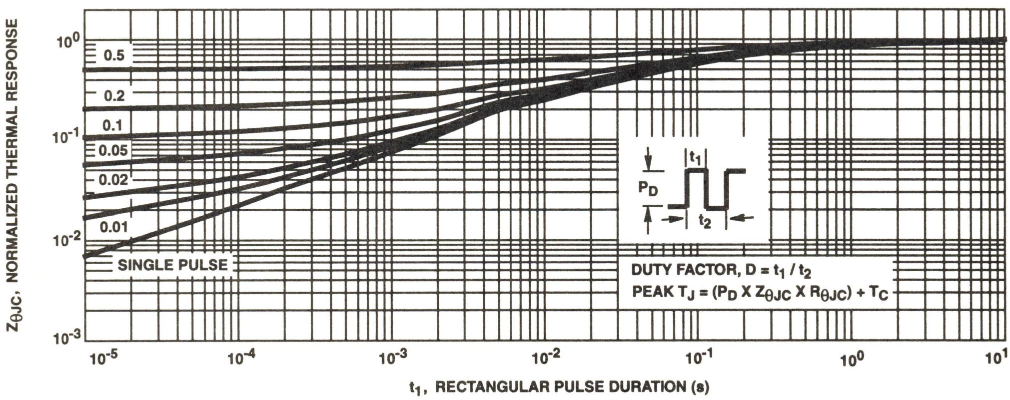


FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Typical Performance Curves (Continued)

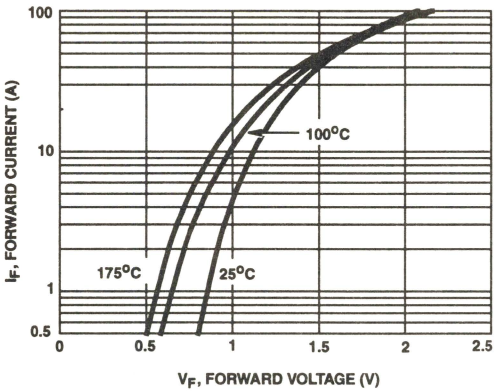


FIGURE 16. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

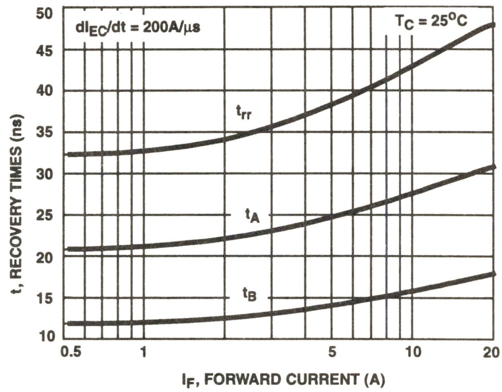
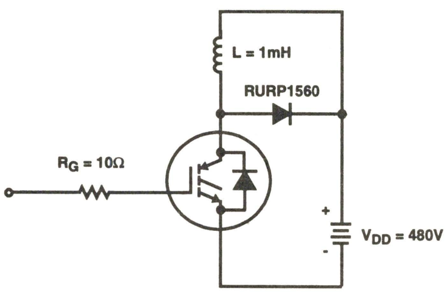


FIGURE 17. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveform



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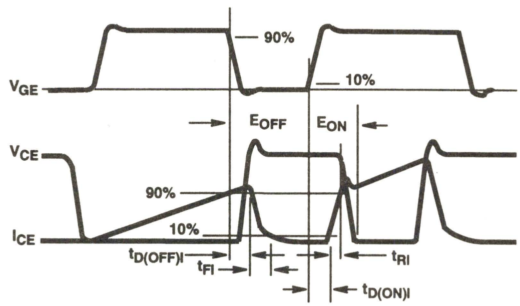

FIGURE 19. SWITCHING TEST WAVEFORMS

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2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

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Operating Frequency Information

Operating frequency information for a typical device (Figure 11) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 3, 5, 6, 9 and 10. The operating frequency plot (Figure 11) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

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f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 11) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 19. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the intepower loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

HARRIS SEMICONDUCTOR

HGTG27N60C3R

January 1997

54A, 600V, Rugged UFS Series N-Channel IGBT

Features

- 54A, 600V, $T_C = 25^oC$
- 600V Switching SOA Capability
- Typical Fall Time at $T_J = 150^oC$ 180ns
- Short Circuit Rating at $T_J = 150^oC$............. 10µs
- Low Conduction Loss

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTG27N60C3R	TO-247	27N60C3R

NOTE: When ordering, use the entire part number.

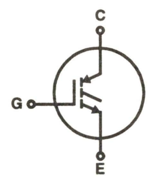
Formerly developmental type TA49048.

Description

This IGBT was designed for optimum performance in the demanding world of motor control operation as well as other high voltage switching applications. This device demonstrates RUGGED performance capability when subjected to harsh SHORT CIRCUIT WITHSTAND TIME (SCWT) conditions. The parts have ULTRAFAST (UFS) switching speed while the on-state conduction losses have been kept at a low level.

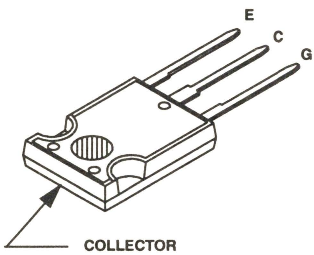
The electrical specifications include typical Turn-On and Turn-Off dv/dt ratings. These ratings and the Turn-On ratings include the effect of the diode, in the test circuit (Figure 16). The data was obtained with the diode at the same T_J as the IGBT under test.

Symbol



Package

JEDEC STYLE TO-247



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4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4245**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTG27N60C3R	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	54	A
At $T_C = 110^oC$	I_{C110}	27	A
Collector Current Pulsed (Note 1)	I_{CM}	108	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Figure 12	SSOA	108A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	208	W
Power Dissipation Derating $T_C > 25^oC$		1.67	W/^{o}C
Reverse Voltage Avalanche Energy	E_{ARV}	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	10	μs

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 440V$, $T_J = 150^oC$, $R_{GE} = 3\Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$, $V_{GE} = 0V$		15	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	μA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	3.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.8	2.2	V
			$T_C = 150^oC$	-	2.1	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$		3.5	5.7	7.5	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA (See Figure 12)	SSOA	$T_J = 150^oC$, $R_G = 3\Omega$ $V_{GE} = 15V$, $V_{CE(PK)} = 600V$ $L = 50\mu H$		108	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	9.0	-	V
On-State Gate Charge	$Q_{g(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{ES}$	$V_{GE} = 15V$	-	156	203	nC
			$V_{GE} = 20V$	-	212	277	nC
Current Turn-On Delay Time	$t_{d(ON)I}$	$T_J = 150^oC$ $I_{CE} = I_{C110}$ $V_{CE(PK)} = 0.8\ BV_{CES}$ $V_{GE} = 15V$ $R_G = 3\Omega$ $L = 1mH$ Diode Used in Test Circuit RURP3060 at 150^{o}C		-	38	-	ns
Current Rise Time	t_{rI}			-	30	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$			-	250	500	ns
Current Fall Time	t_{fI}			-	180	400	ns
Turn-Off Voltage dv/dt (Note 3)	dV_{CE}/dt			-	2	-	V/ns
Turn-On Voltage dv/dt (Note 3)	dV_{CE}/dt			-	7	-	V/ns
Turn-On Energy (Note 4)	E_{ON}			-	2.3	-	mJ
Turn-Off Energy (Note 5)	E_{OFF}			-	2.0	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	-	0.6	^{o}C/W

NOTES:

3. dV_{CE}/dt depends on the diode used and the temperature of the diode. dV_{CE}/dt is measured from 90% to 10% of the voltage.
4. Turn-On Energy Loss (E_{ON}) includes diode losses and is defined as the integral of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the collector voltage equals V_{CE}(ON). This value of E_{ON} was obtained with a RURP3060 diode at $T_J = 150^oC$. A different diode or temperature will result in a different E_{ON}. For example with diode at $T_J = 25^oC$ E_{ON} is about one half the value at 150^{o}C.
5. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

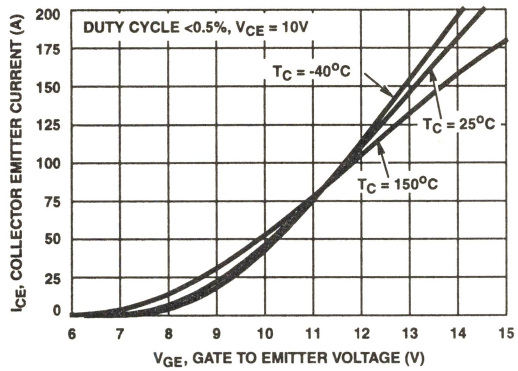

FIGURE 1. TRANSFER CHARACTERISTICS

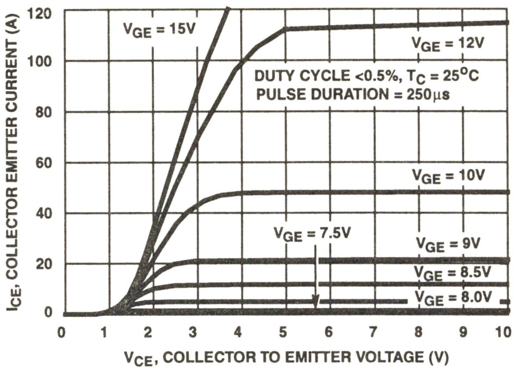

FIGURE 2. SATURATION CHARACTERISTICS

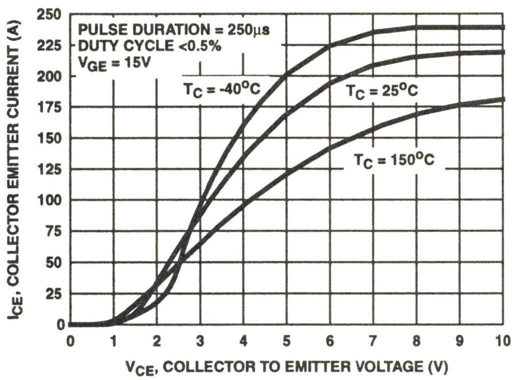

FIGURE 3. COLLECTOR EMITTER ON-STATE VOLTAGE

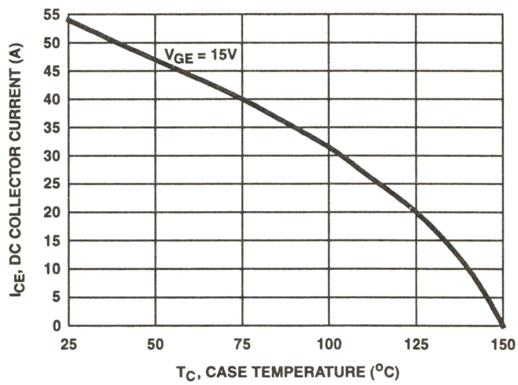

FIGURE 4. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

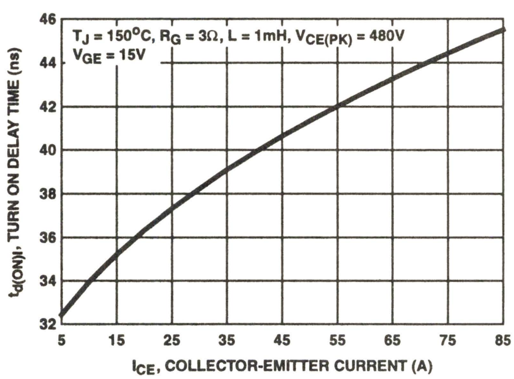

FIGURE 5. TURN ON DELAY TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

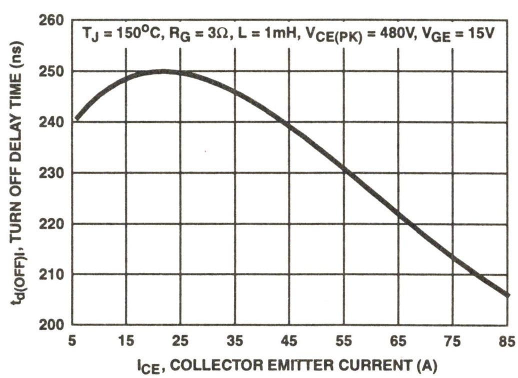

FIGURE 6. TURN OFF DELAY TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

Typical Performance Curves (Continued)

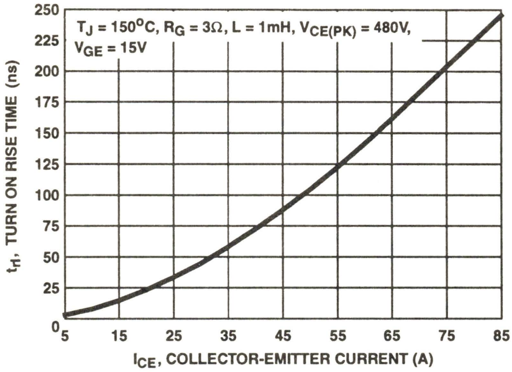

FIGURE 7. TURN ON RISE TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

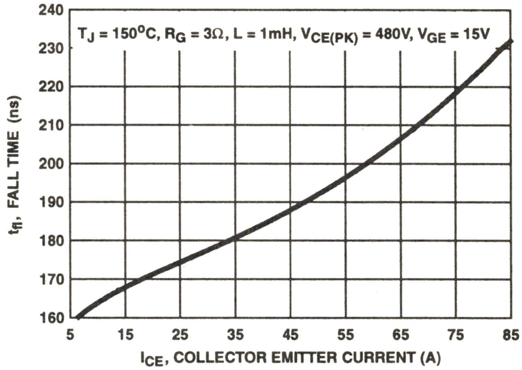

FIGURE 8. TURN OFF FALL TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

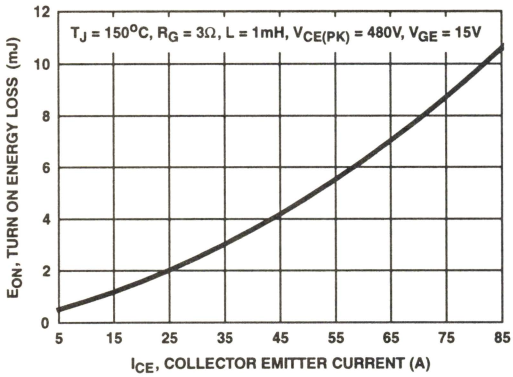

FIGURE 9. TURN ON ENERGY LOSS AS A FUNCTION OF COLLECTOR EMITTER CURRENT

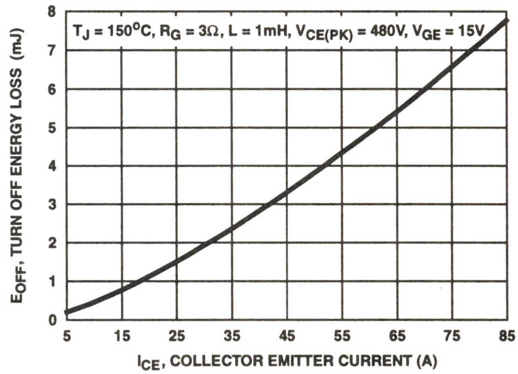

FIGURE 10. TURN OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR EMITTER CURRENT

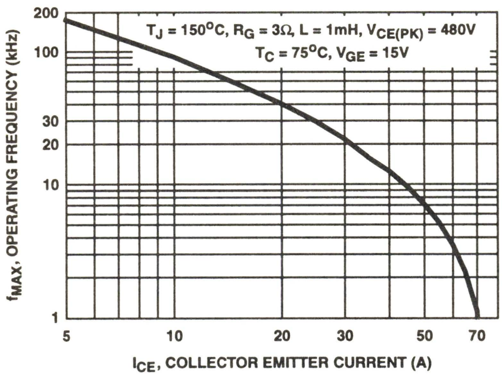

FIGURE 11. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR EMITTER CURRENT

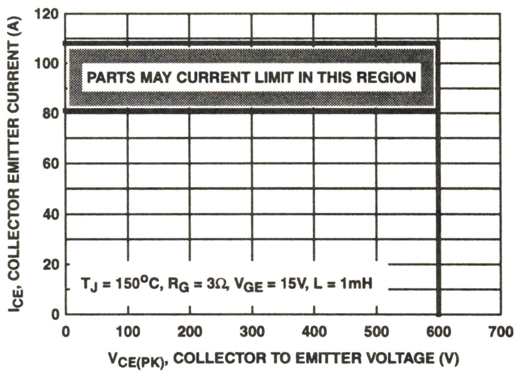

FIGURE 12. SWITCHING SAFE OPERATING AREA

Typical Performance Curves (Continued)

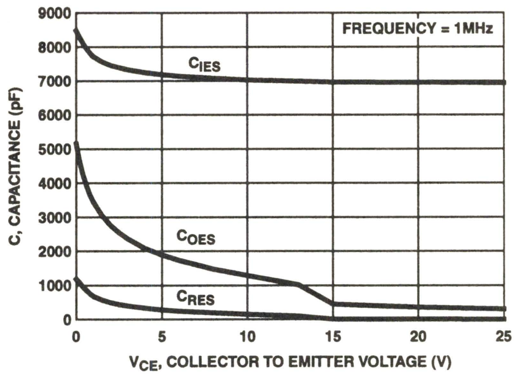

FIGURE 13. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

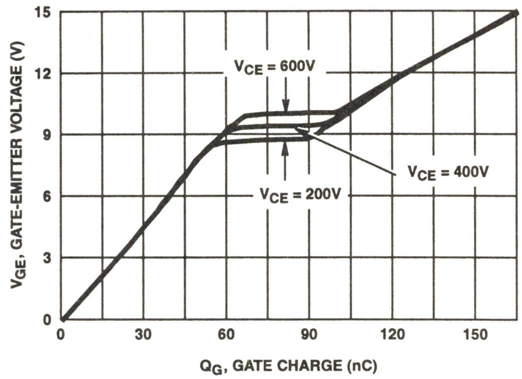

FIGURE 14. GATE CHARGE WAVEFORMS

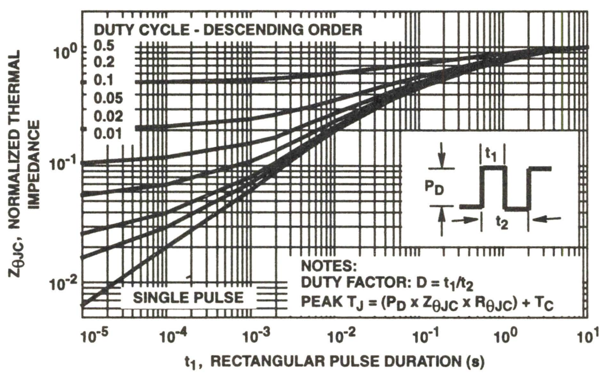

FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Test Circuit and Waveform

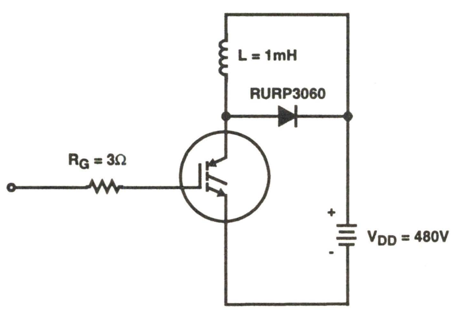

FIGURE 16. INDUCTIVE SWITCHING TEST CIRCUIT

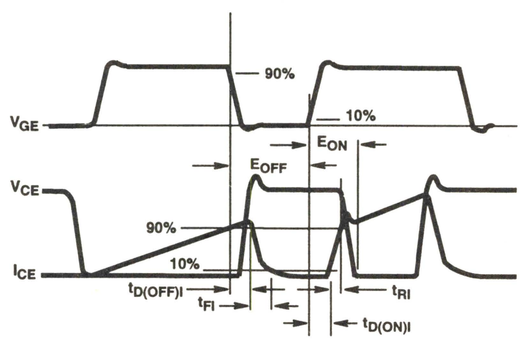

FIGURE 17. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

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Operating Frequency Information

Operating frequency information for a typical device (Figure 11) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 3, 5, 6, 9 and 10. The operating frequency plot (Figure 11) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 17. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 11) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$ shown in Figure 17.

E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$).

HARRIS SEMICONDUCTOR

HGTG27N60C3DR

54A, 600V, Rugged UFS Series N-Channel IGBT with Anti-Parallel Ultrafast Diode

January 1997

Features

- **54A, 600V, $T_C = 25^oC$**
- **600V Switching SOA Capability**
- **Typical Fall Time at $T_J = 150^oC$ 200ns**
- **Short Circuit Rating at $T_J = 150^oC$. 10μs**
- **Low Conduction Loss**

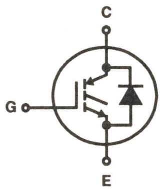
Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTG27N60C3DR	TO-247	27N60C3DR

NOTE: When ordering, use the entire part number.

Symbol

N-CHANNEL ENHANCEMENT MODE



Description

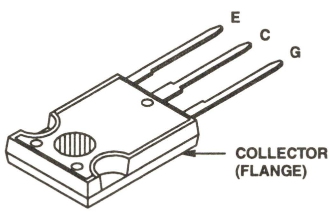
This IGBT was designed for optimum performance in the demanding world of motor control operation as well as other high voltage switching applications. This device demonstrates RUGGED performance capability when subjected to harsh SHORT CIRCUIT WITHSTAND TIME (SCWT) conditions. The parts have ULTRAFAST (UFS) switching speed while the on-state conduction losses have been kept at a low level.

The electrical specifications include typical Turn-On and Turn-Off dv/dt ratings. These ratings and the turn-on ratings include the effect of the diode in the test circuit (Figure 18). The data was obtained with the diode at the same T_J as the IGBT under test. The IGBT was formerly developmental type 49048. The diode used in anti-parallel with the IGBT was formerly developmental type 49214.

The IGBT diode combination was formerly developmental type TA49013.

Package

JEDEC STYLE TO-247



HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4262**

Absolute Maximum Ratings $T_C = 25^o$ Unless Otherwise Specified

		HGTG27N60C3DR	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	54	A
At $T_C = 110^oC$	I_{C110}	27	A
Collector Current Pulsed (Note 1)	I_{CM}	108	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, (Figure 12)	SSOA	108A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	208	W
Power Dissipation Derating $T_C > 25^oC$		1.67	W/^{o}C
Reverse Voltage Avalanche Energy	E_{ARV}	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to 150	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	10	µs

NOTES:

1. Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 440V$, $T_J = 150^oC$, $R_{GE} = 3\Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$, $V_{GE} = 0V$		15	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
			$T_C = 150^oC$	-	-	3.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	1.8	2.2	V
			$T_C = 150^oC$	-	2.1	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$		3.5	5.7	7.5	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA (See Figure 12)	SSOA	$T_J = 150^oC$, $R_G = 3\Omega$, $L = 50\mu H$, $V_{GE} = 15V$, $V_{CE(PK)} = 600V$		108	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	9.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{ES}$	$V_{GE} = 15V$	-	156	203	nC
			$V_{GE} = 20V$	-	212	277	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 3\Omega$, $L = 1mH$, Diode used in test circuit RURP3060 at 150^{o}C		-	38	-	ns
Current Rise Time	t_{RI}			-	30	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	250	500	ns
Current Fall Time	t_{FI}			-	200	400	ns
Turn-Off Voltage dv/dt (Note 3)	dV_{CE}/dt			-	2	-	V/ns
Turn-On Voltage dv/dt (Note 3)	dV_{CE}/dt			-	7	-	V/ns
Turn-On Energy (Note 4)	E_{ON}			-	2.3	-	mJ
Turn-Off Energy (Note 5)	E_{OFF}			-	2.0	-	mJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 27A$		-	-	1.5	V

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
Diode Reverse Recovery Time	t_{rr}	$I_{EC} = 1A$, $dI_{EC}/dt = 200A/\mu s$	-	-	55	ns
		$I_{EC} = 27A$, $dI_{EC}/dt = 200A/\mu s$	-	-	60	ns
Thermal Resistance	$R_{\theta JC}$	IGBT	-	-	0.6	$^oC/W$
		Diode	-	-	1.25	$^oC/W$

NOTES:

3. dV_{CE}/dt depends on the diode used and the temperature of the diode.
4. Turn-On Energy Loss (E_{ON}) includes losses due to the diode recovery and is defined as the integral of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the collector voltage equals $V_{CE(SAT)}$. This value of E_{ON} was obtained with a RURP3060 diode at $T_J = 150^oC$. A different diode or temperature will result in a different E_{ON}. For example, with diode at $T_J = 25^oC$ E_{ON} is about one half the value at 150^oC.
5. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC standard No. 24-1 Method for measurement of power device turn-off switching loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

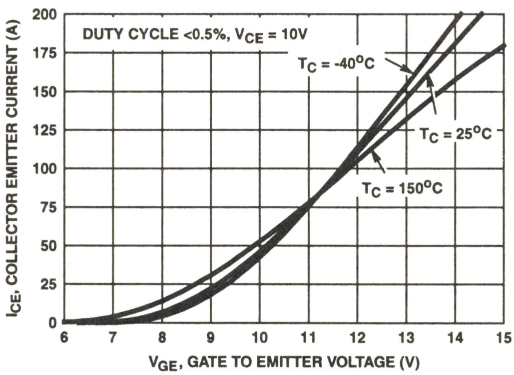


FIGURE 1. TRANSFER CHARACTERISTICS

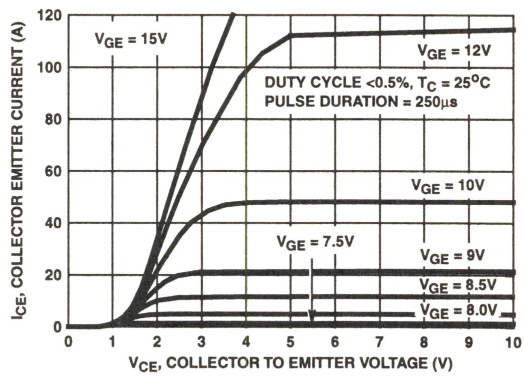


FIGURE 2. SATURATION CHARACTERISTICS

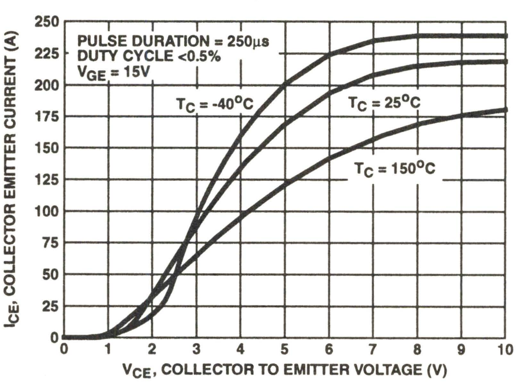


FIGURE 3. COLLECTOR EMITTER ON STATE VOLTAGE

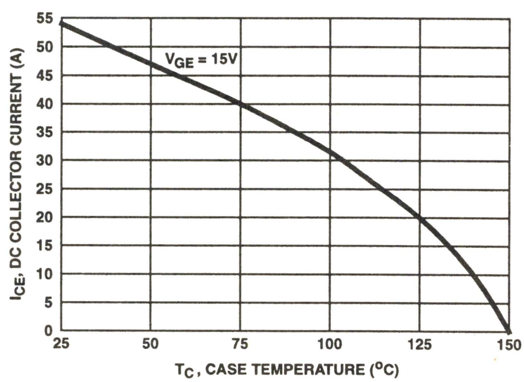


FIGURE 4. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

Typical Performance Curves (Continued)

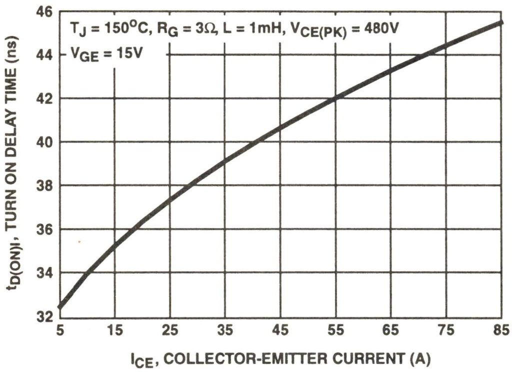


FIGURE 5. TURN ON DELAY TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

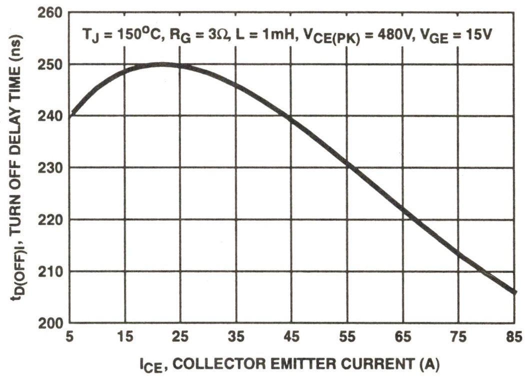


FIGURE 6. TURN OFF DELAY TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

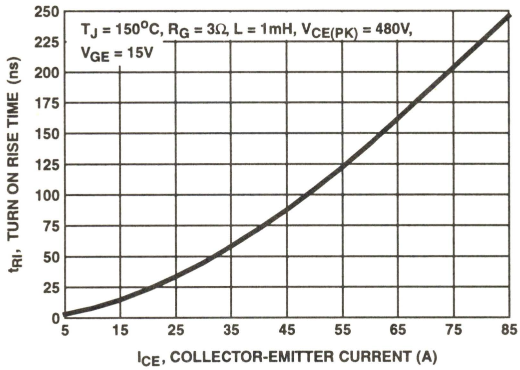


FIGURE 7. TURN ON RISE TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

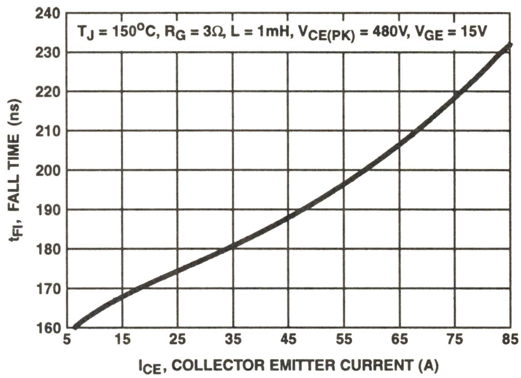


FIGURE 8. TURN OFF FALL TIME AS A FUNCTION OF COLLECTOR EMITTER CURRENT

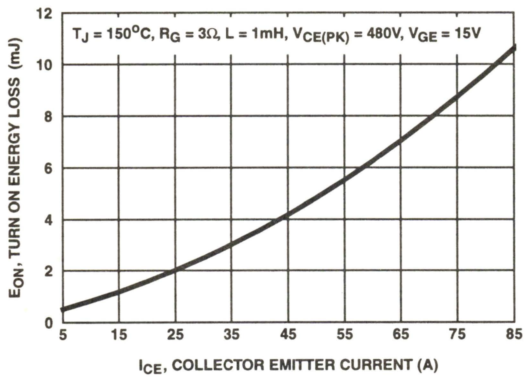


FIGURE 9. TURN ON ENERGY LOSS AS A FUNCTION OF COLLECTOR EMITTER CURRENT

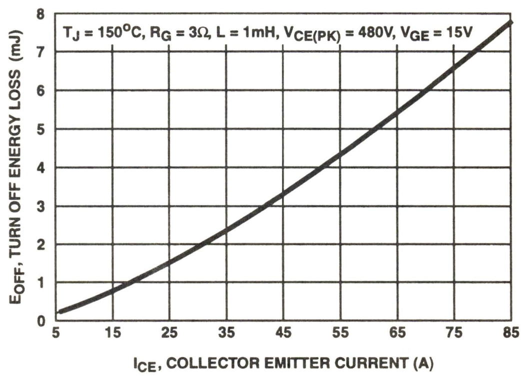


FIGURE 10. TURN OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR EMITTER CURRENT

Typical Performance Curves (Continued)

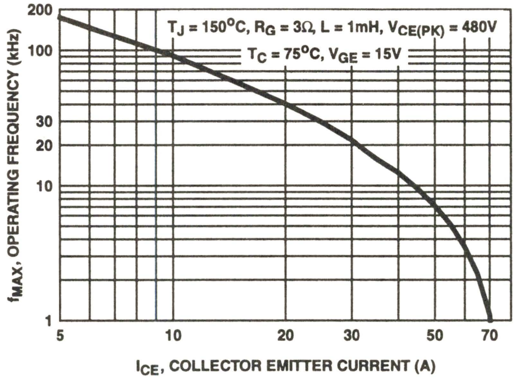


FIGURE 11. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR EMITTER CURRENT

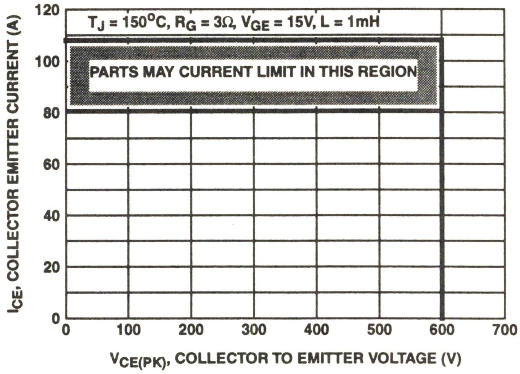


FIGURE 12. SWITCHING SAFE OPERATING AREA

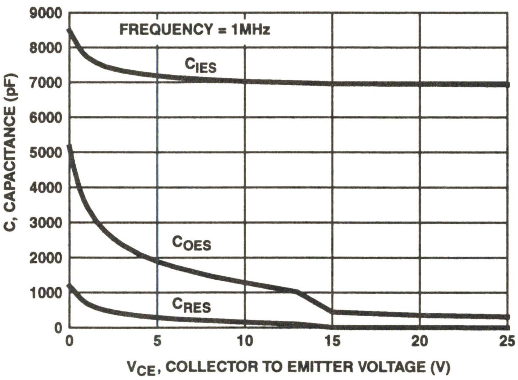


FIGURE 13. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

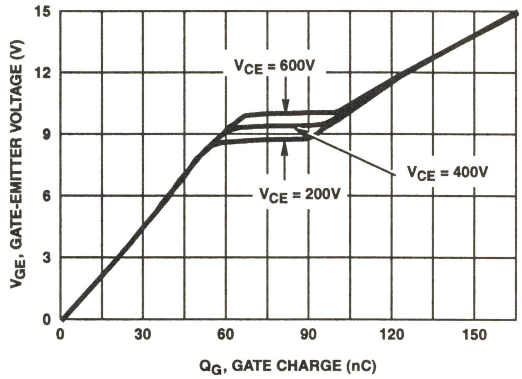


FIGURE 14. GATE CHARGE WAVEFORMS

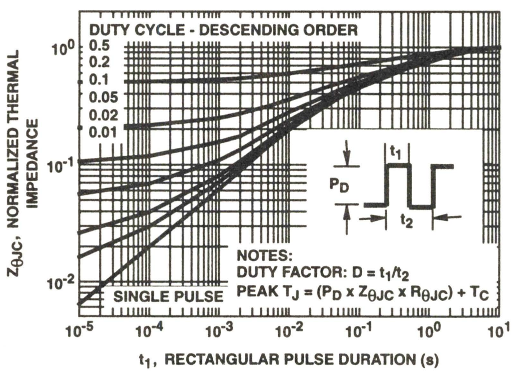


FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

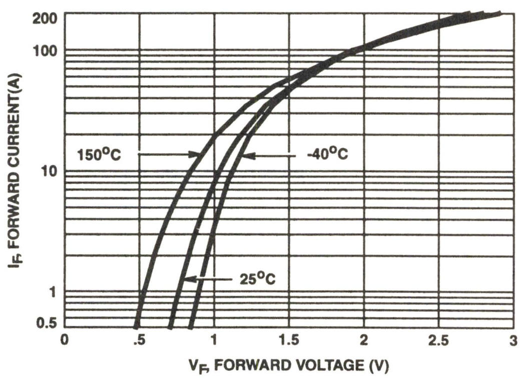


FIGURE 16. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

Typical Performance Curves (Continued)

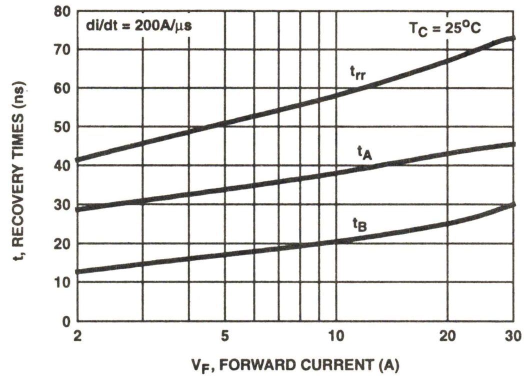


FIGURE 17. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveform

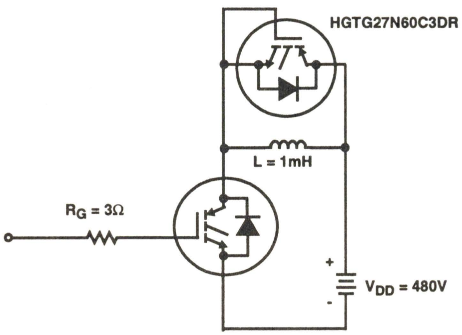


FIGURE 18. INDUCTIVE SWITCHING TEST CIRCUIT

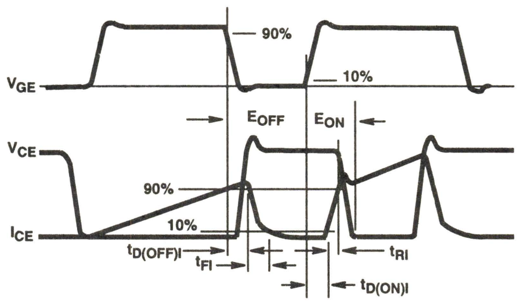


FIGURE 19. SWITCHING TEST WAVEFORMS

5
RUGGED UFS SERIES

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

ECCOSORBD™ is a Trademark of Emerson and Cumming, Inc.

Operating Frequency Information

Operating frequency information for a typical device (Figure 11) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 3, 5, 6, 9 and 10. The operating frequency plot (Figure 11) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 17. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 11) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 17. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$).

IGBT UFS SERIES SUPPLEMENT

6

1200 VOLT UFS SERIES IGBTs

PAGE

1200 Volt UFS Series IGBT Data Sheets

HGTP15N120C3 35A, 1200V, UFS Series N-Channel IGBT 6-3

HGTG15N120C3D 35A, 1200V, UFS Series N-Channel IGBT 6-10

HGTP15N120C3

January 1997

35A, 1200V, UFS Series N-Channel IGBT

Features

- 35A, 1200V $T_C = 25^oC$
- 1200V Switching SOA Capability
- Typical Fall Time .... 350ns at $T_J = 150^oC$
- Short Circuit Rating
- Low Conduction Loss

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTP15N120C3	TO-220AB	15N120C3

NOTE: When ordering, use the entire part number.

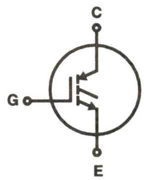
Description

The HGTP15N120C3 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25°C and 150°C.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

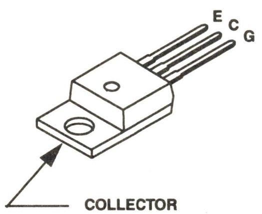
Formerly Developmental Type TA49145.

Symbol



Package

JEDEC TO-220AB



HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

6

1200V UFS SERIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4244.1**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTP15N120C3	UNITS
Collector-Emitter Voltage	BV_{CES}	1200	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	35	A
At $T_C = 110^oC$	I_{C110}	15	A
Collector Current Pulsed (Note 1)	I_{CM}	120	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Fig. 14	SSOA	15A at 1200V	
Power Dissipation Total at $T_C = 25^oC$	P_D	164	W
Power Dissipation Derating $T_C > 25^oC$		1.32	W/^{o}C
Reverse Voltage Avalanche Energy	E_{ARV}	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	6	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	25	µs

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 720V$, $T_J = 125^oC$, $R_{GE} = 25\Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		1200	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$, $V_{GE} = 0V$		15	25	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	3.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	2.3	3.5	V
			$T_C = 150^oC$	-	2.4	3.2	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = 25^oC$	4.0	5.6	7.5	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 10\Omega$, $V_{GE} = 15V$, $L = 1mH$	$V_{CE(PK)} = 960V$	40	-	-	A
			$V_{CE(PK)} = 1200V$	15	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8.8	-	V
On-State Gate Charge	$Q_{g(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{ES}$	$V_{GE} = 15V$	-	75	100	nC
			$V_{GE} = 20V$	-	100	130	nC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Turn-On Delay Time	$t_{d(ON)I}$	$T_J = 150^oC$ $I_{CE} = I_{C110}$ $V_{CE(PK)} = 0.8\ BV_{CES}$ $V_{GE} = 15V$ $R_G = 10\Omega$ $L = 1mH$	-	17	-	ns
Current Rise Time	t_{RI}		-	25	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$		-	470	550	ns
Current Fall Time	t_{FI}		-	350	400	ns
Turn-On Energy	E_{ON}		-	2100	-	µJ
Turn-Off Energy (Note 3)	E_{OFF}		-	4700	-	µJ
Thermal Resistance	$R_{\theta JC}$		-	-	0.76	$^oC/W$

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include losses due to diode recovery.

Typical Performance Curves

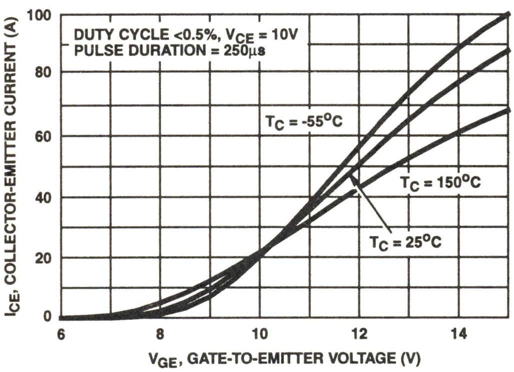


FIGURE 1. TRANSFER CHARACTERISTICS

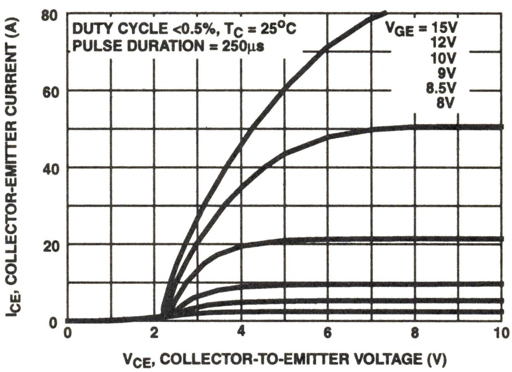


FIGURE 2. SATURATION CHARACTERISTICS

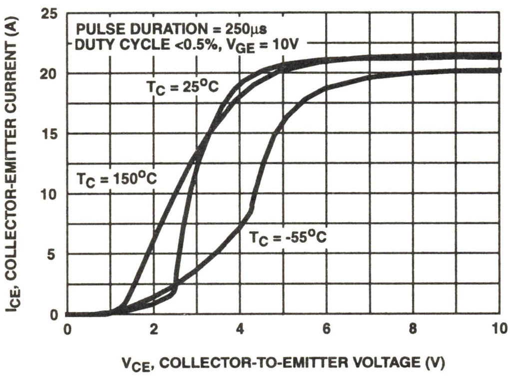


FIGURE 3. COLLECTOR-EMITTER ON-STATE VOLTAGE

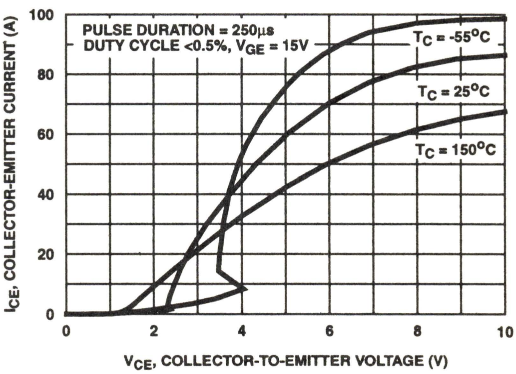


FIGURE 4. COLLECTOR-EMITTER ON-STATE VOLTAGE

Typical Performance Curves (Continued)

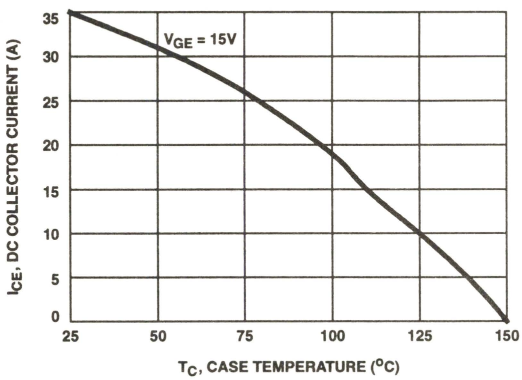


FIGURE 5. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

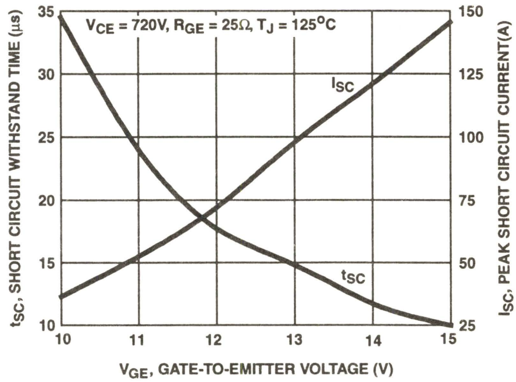


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

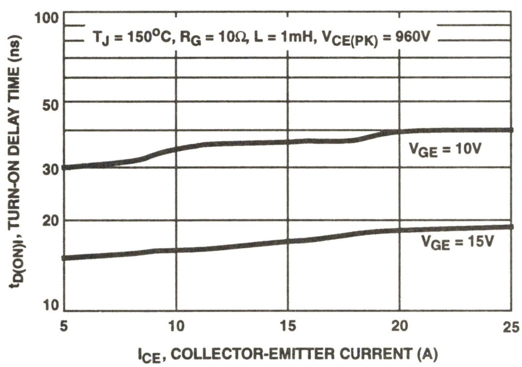


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

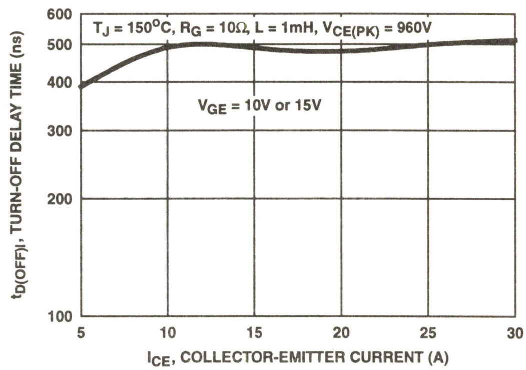


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

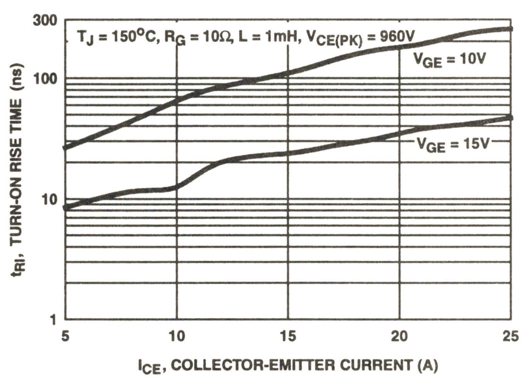


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

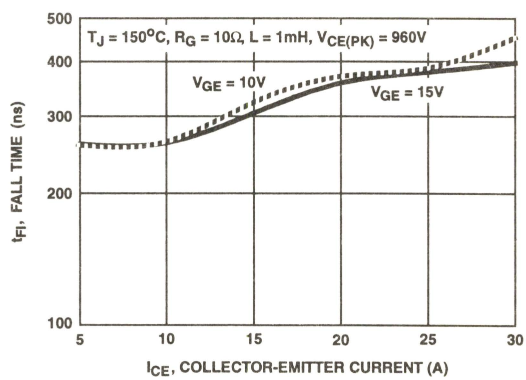


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

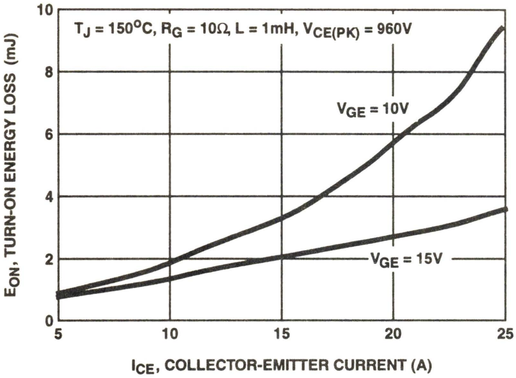
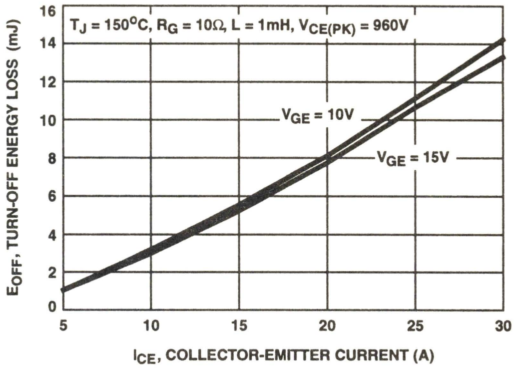


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT



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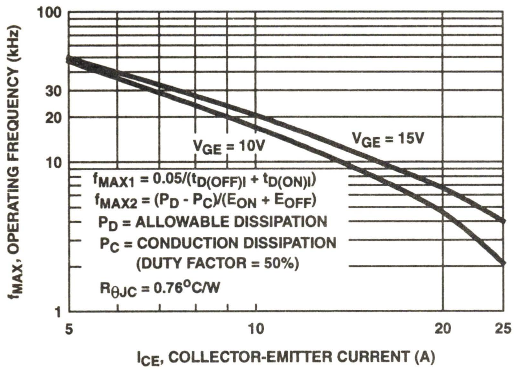
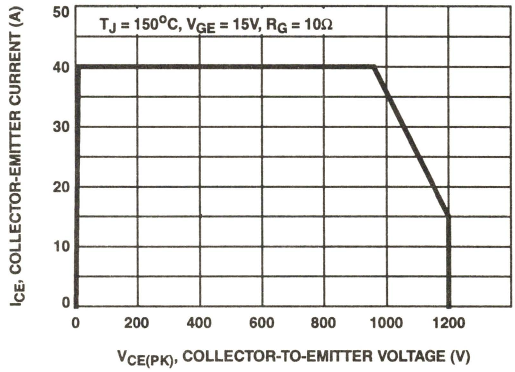


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT



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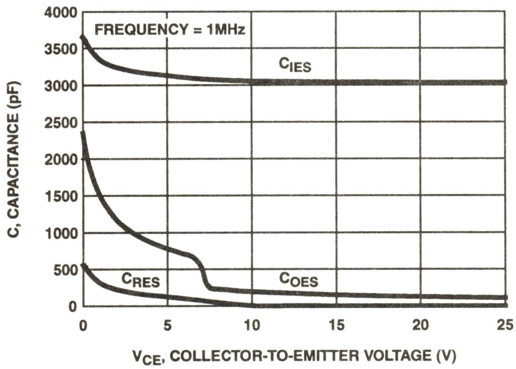


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

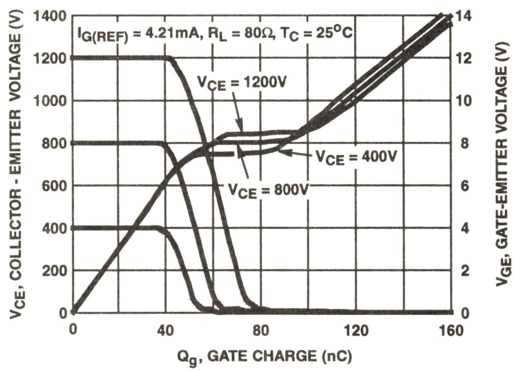
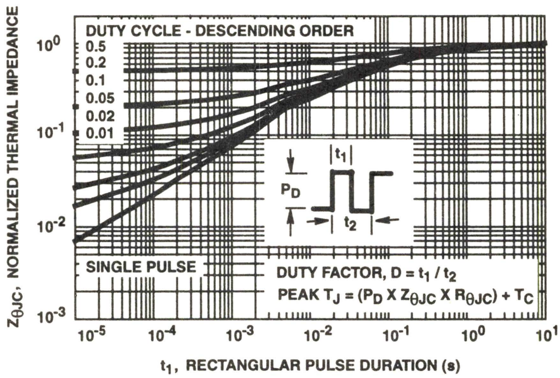


FIGURE 16. GATE CHARGE WAVEFORMS

Typical Performance Curves (Continued)



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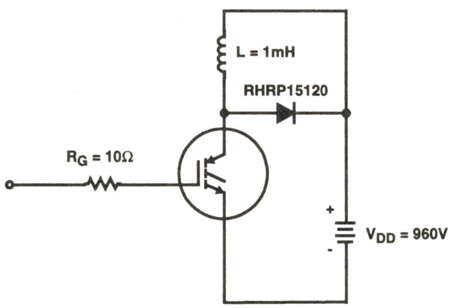

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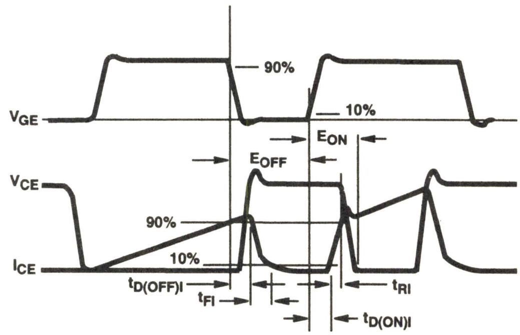

FIGURE 19. SWITCHING TEST WAVEFORMS

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Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 19. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 19. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

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HARRIS SEMICONDUCTOR

HGTG15N120C3D

December 1996

35A, 1200V, UFS Series N-Channel IGBT

Features

- 35A, 1200V at $T_C = 25^oC$
- 1200V Switching SOA Capability
- Typical Fall Time at $T_J = 150^oC$ 350ns
- Short Circuit Rating
- Low Conduction Loss

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTG15N120C3D	TO-247	15N120C3D

NOTE: When ordering, use the entire part number.

Formerly Developmental Type TA49133.

Description

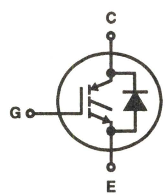
The HGTG15N120C3D is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. This device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between 25^oC and 150^oC.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

The diode used in anti-Parallel with the IGBT is the same as the RURP15120. The IGBT was formerly development type TA49145.

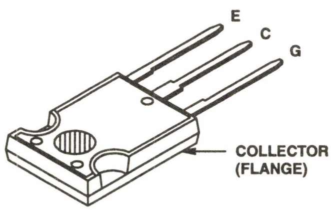
Symbol

N-CHANNEL ENHANCEMENT MODE



Packaging

JEDEC STYLE TO-247



HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4267**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HGTG15N120C3D	UNITS
Collector-Emitter Voltage	BV_{CES}	1200	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	35	A
At $T_C = 110^oC$	I_{C110}	15	A
Collector Current Pulsed (Note 1)	I_{CM}	120	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = 150^oC$, Figure 14	SSOA	15A at 1200V	
Power Dissipation Total at $T_C = 25^oC$	P_D	164	W
Power Dissipation Derating $T_C > 25^oC$		1.32	W/^{o}C
Reverse Voltage Avalanche Energy	E_{ARV}	100	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	6	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	25	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_J = 125^oC$, $R_{GE} = 25\Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		1200	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$, $V_{GE} = 0V$		15	25	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = 25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = 150^oC$	-	-	3.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = 25^oC$	-	2.3	3.5	V
			$T_C = 150^oC$	-	2.4	3.2	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$		4.0	5.6	7.5	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Switching SOA	SSOA	$T_J = 150^oC$, $R_G = 10\Omega$, $V_{GE} = 15V$, $L = 1mH$	$V_{CE(PK)} = 960V$	40	-	-	A
			$V_{CE(PK)} = 1200V$	15	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8.8	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	75	100	nC
			$V_{GE} = 20V$	-	100	130	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = 150^oC$, $I_{CE} = I_{C110}$, $V_{CE(PK)} = 0.8\ BV_{CES}$, $V_{GE} = 15V$, $R_G = 10\Omega$, $L = 1mH$		-	17	-	ns
Current Rise Time	t_{RI}			-	25	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	470	550	ns
Current Fall Time	t_{FI}			-	350	400	ns
Turn-On Energy (Note 3)	E_{ON}			-	2100	-	µJ
Turn-Off Energy (Note 3)	E_{OFF}			-	4700	-	µJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 15A$		-	-	3.2	V
Diode Reverse Recovery Time	t_{rr}	$I_{EC} = 1A$, $dI_{EC}/dt = 200A/\mu s$		-	-	65	ns
		$I_{EC} = 15A$, $dI_{EC}/dt = 200A/\mu s$		-	-	75	ns
Thermal Resistance	$R_{\theta JC}$	IGBT		-	-	0.76	^{o}C/W
		Diode		-	-	1.5	^{o}C/W

NOTE:

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTG15N120C3D was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On Energy loss (E_{ON}) includes losses due to the diode recovery.

Typical Performance Curves

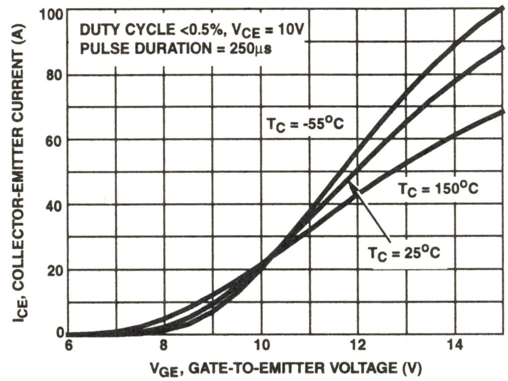


FIGURE 1. TRANSFER CHARACTERISTICS

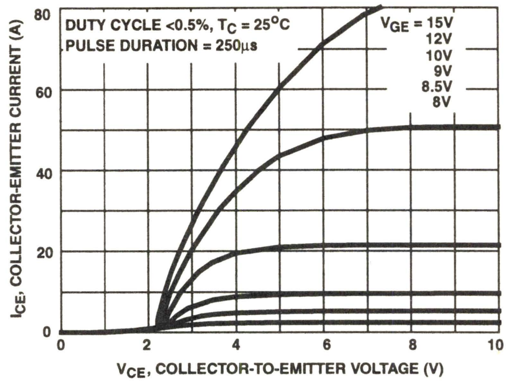


FIGURE 2. SATURATION CHARACTERISTICS

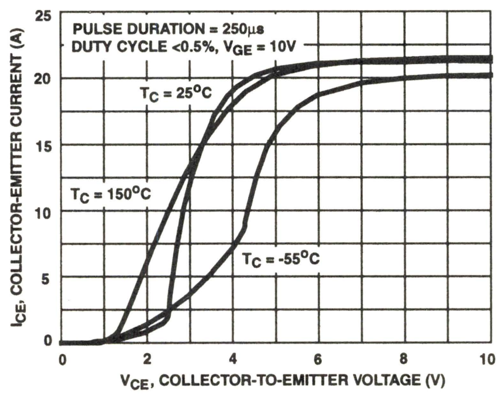


FIGURE 3. COLLECTOR-EMITTER ON-STATE VOLTAGE

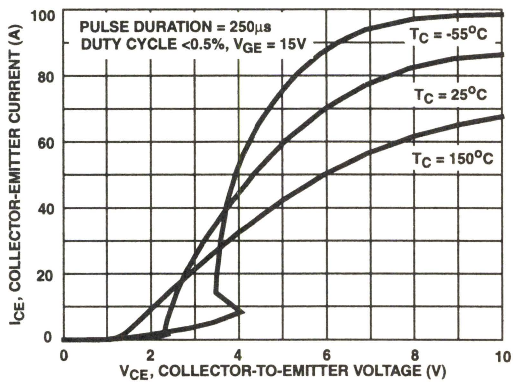


FIGURE 4. COLLECTOR-EMITTER ON-STATE VOLTAGE

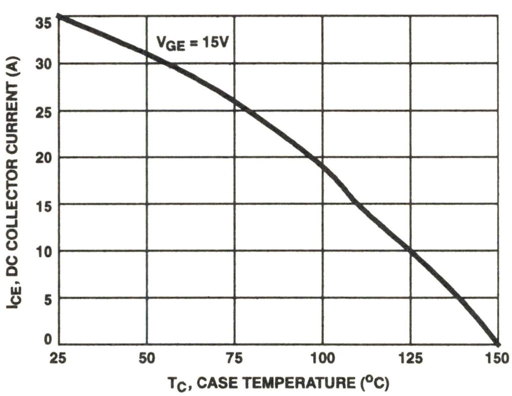


FIGURE 5. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

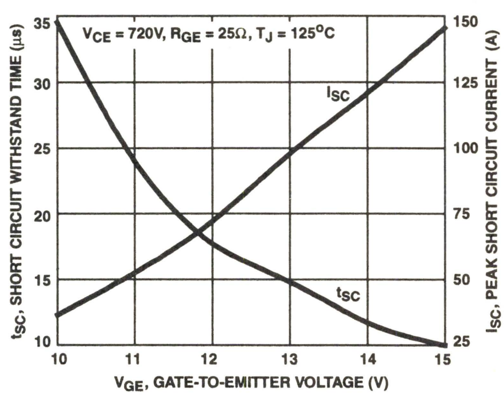


FIGURE 6. SHORT CIRCUIT WITHSTAND TIME

Typical Performance Curves (Continued)

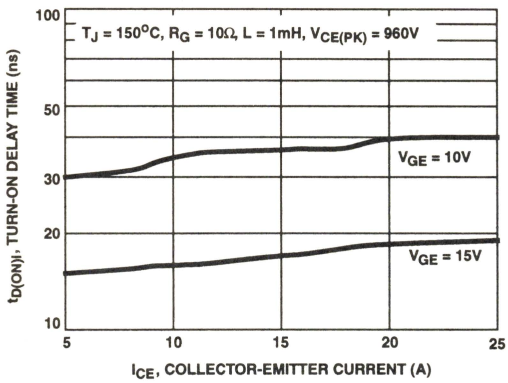


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

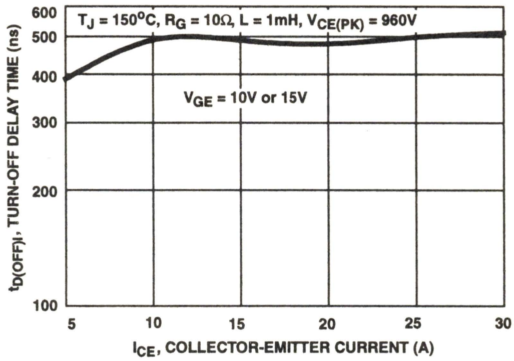


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

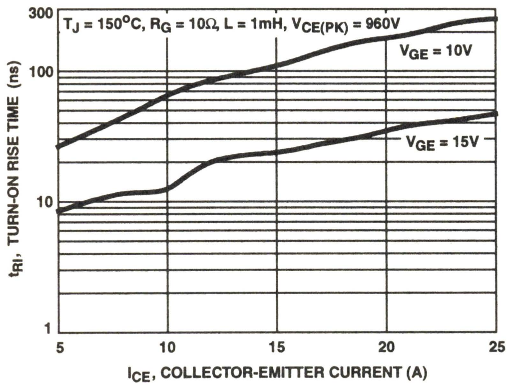


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

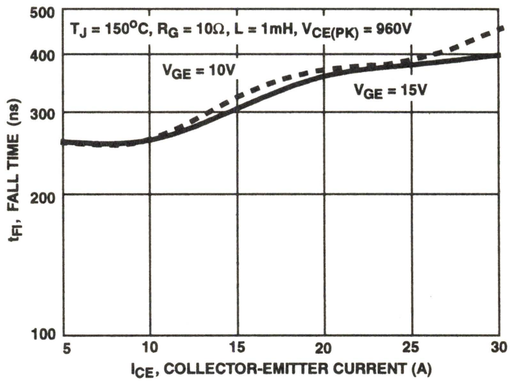


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

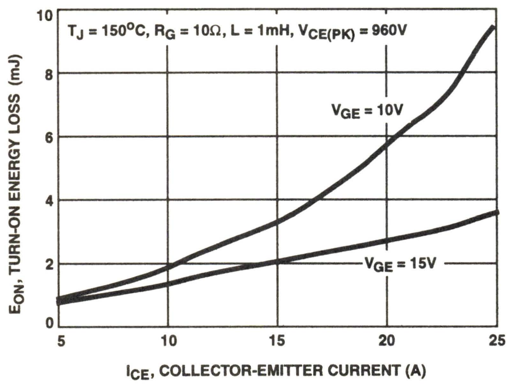


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

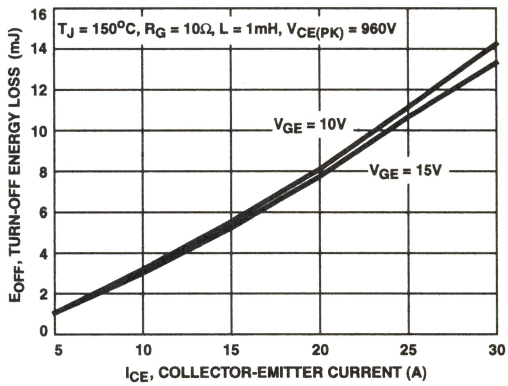


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

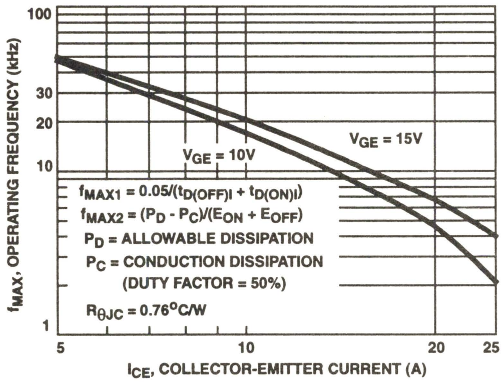


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

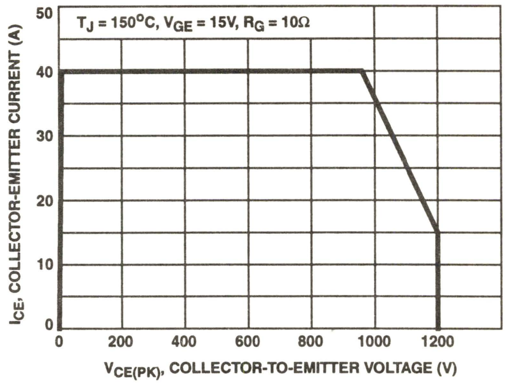


FIGURE 14. SWITCHING SAFE OPERATING AREA

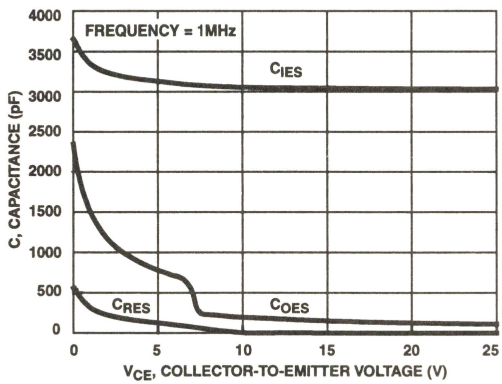


FIGURE 15. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

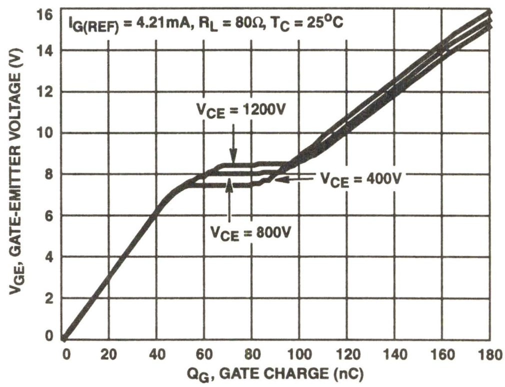


FIGURE 16. GATE CHARGE WAVEFORM

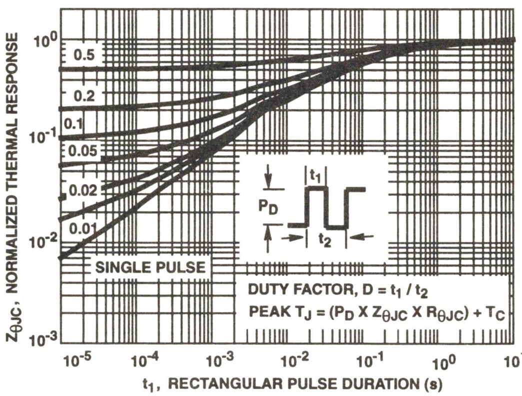


FIGURE 17. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Typical Performance Curves (Continued)

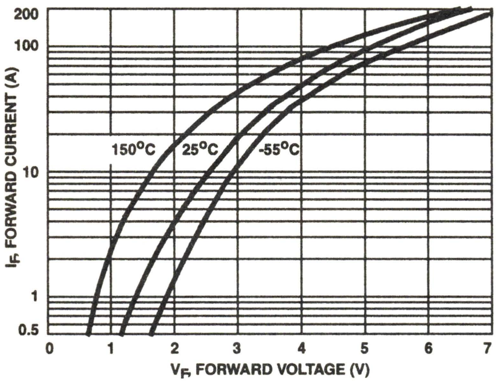


FIGURE 18. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

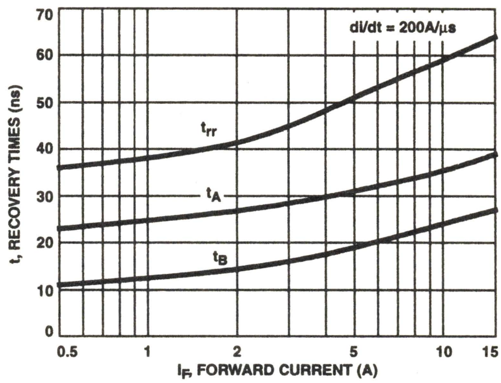


FIGURE 19. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveform

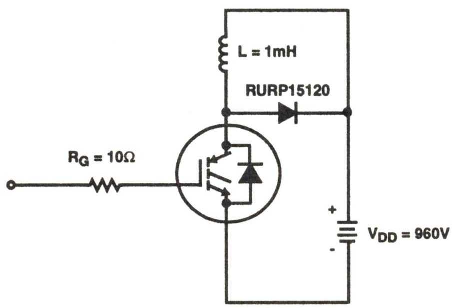


FIGURE 20. INDUCTIVE SWITCHING TEST CIRCUIT

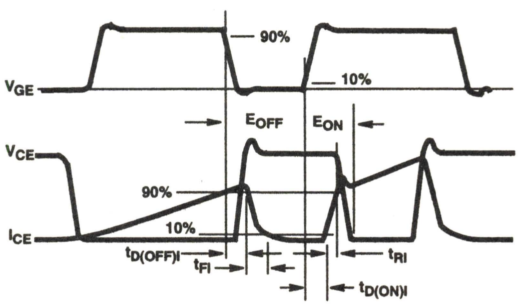


FIGURE 21. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

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Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 21. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 21. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

IGBT UFS SERIES SUPPLEMENT 7

HARRIS QUALITY AND RELIABILITY

PAGE

Quality and Reliability Assurance 7-3
In-Process Quality Control 7-3
Control of Outgoing Product 7-3
Reliability Assurance 7-3
The Reliability Program 7-3

Quality and Reliability Assurance

The ability to build and maintain the high levels of quality and reliability today, depends on inherent design and process capability, and not the degree of test and inspection. Both the design and production facilities for Power MOSFETs are totally new, with state-of-the-art equipment and process techniques which deliver this needed capability.

In-Process Quality Control

All critical phases of the highly automated power MOSFET manufacturing cycle have been characterized with respect to their intrinsic variability. Statistical limits have been established to give warning of abnormal process trends and fluctuations, based on this intrinsic capability. These limits are constantly tightened as the process improves and are well within the engineering specifications. The emphasis at Harris is to employ statistical methods at the point of control, rather than an inspection point at the end of a process.

Control of Outgoing Product

The quality control lot acceptance sampling of finished product is performed after manufacturing has performed 100% inspection of all specified electrical characteristics. This, combined with tight parameter distributions gained through process control and inherent design capability, the average outgoing quality level (AOQ) to the customer has been in the order of 1ppm (0.01%).

Reliability Assurance

Harris Semiconductor has a world-wide reliability program that helps to shape the direction of new product development, assures that the reliability level is maintained throughout the production cycle, and develops specific models to predict the reliability in the end-use application. In order to meet these objectives, a reliability facility is maintained at each manufacturing location for real-time feedback. A centralized reliability engineering organization develops all new test methods and supports new product/process development. Each group is fully trained in the reliability and applied statistics disciplines, as well as failure analysis, and are responsible for using these techniques to monitor and improve product capability.

The Reliability Program

The reliability-assurance program operates at all stages of production, using the following four-pronged approach:

Product Design and Development

During early development, initial product lots are characterized through accelerated reliability tests which establish the product capability. Once the design had been fine-tuned, multiple production runs are initiated and samples are subjected to a full range of standardized accelerated tests. All lots must meet pre-established reliability standards before any new design or process can be released for production.

Real Time Indicators (RTI)

RTI's are short-duration accelerated-stress tests used to control the occurrence of specific failure mechanisms that can significantly affect product reliability. The stress levels are designed to induce failures, so that product-capability shifts can be detected and corrected. They are performed weekly at each manufacturing location. In this real-time method of determining reliability, a continuous flow of data is provided to indicate how well the manufacturing process is performing product.

TABLE 1. TYPICAL MOSFET RTI TESTS

TEST	CONDITIONS	PACKAGE	TYPICAL DURATION
Power Cycling	PD = 4.75W T_J = +35^{o}C - 175^{o}C (approx.)	Plastic	10 - 15K Cycles
D-S Bias Life	T_A = +150^{o}C 80% of Drain Source	All	168 Hours
G-S Bias Life	G - S = 16V T_A = +150^{o}C	All	168 Hours

Requalification Program (RQP)

Each product is requalified every six to twelve months to the same matrix of tests required for the initial production release. This operation measures the changes in the total capability of each MOSFET family to meet the original reliability design objectives. Table 2 is typical of the data generated for RQP.

Reliability Data

Current reliability data can be found on the world wide web at http://www.mtp.semi.harris.com/

IGBT UFS SERIES SUPPLEMENT 8

PACKAGING INFORMATION

PAGE

Power Packages

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TO-220AB (Alternate Version) 8-4
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TO-251AA 8-6
TO-252AA 8-7
TO-252AA (Tape and Reel) 8-8
TO-262AA 8-9
TO-263AB 8-10
TO-263AB (Tape and Reel) 8-11

Handling Precautions for Insulated Gate Bipolar Transistors (IGBTs)

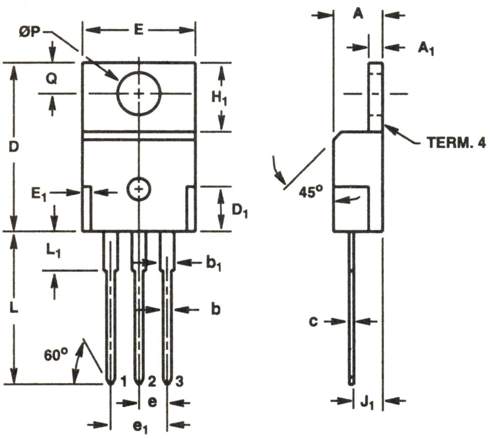
Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "† ECCOSORBD LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.

† Trademark Emerson and Cumming, Inc.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



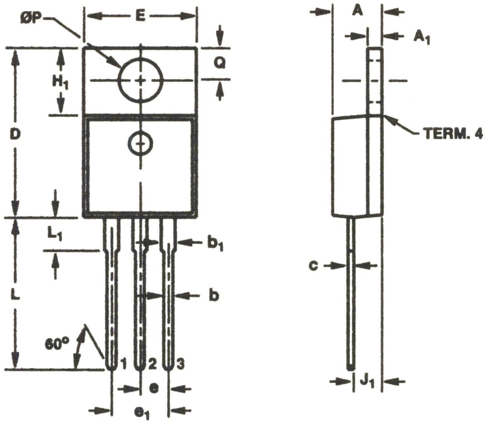
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

TO-220AB (Alternate Version)

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



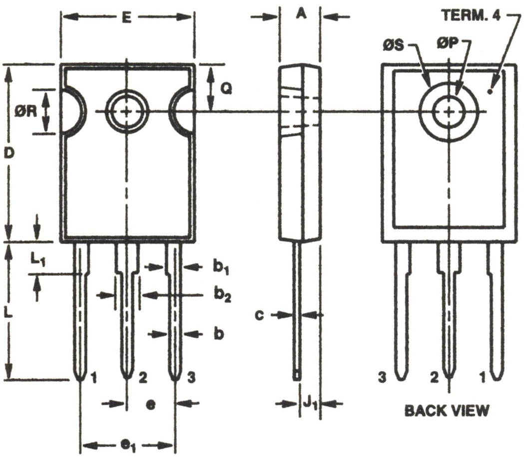
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	2, 4
b	0.030	0.034	0.77	0.86	2, 4
b_1	0.045	0.055	1.15	1.39	2, 4
c	0.018	0.022	0.46	0.55	2, 4
D	0.590	0.610	14.99	15.49	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	3
ØP	0.149	0.153	3.79	3.88	-
Q	0.105	0.115	2.66	2.92	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Dimension (without solder).
3. Solder finish uncontrolled in this area.
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 10-95.

TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



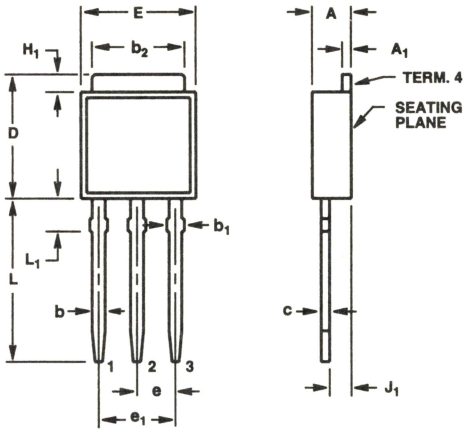
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

TO-251AA

3 LEAD JEDEC TO-251AA PLASTIC PACKAGE



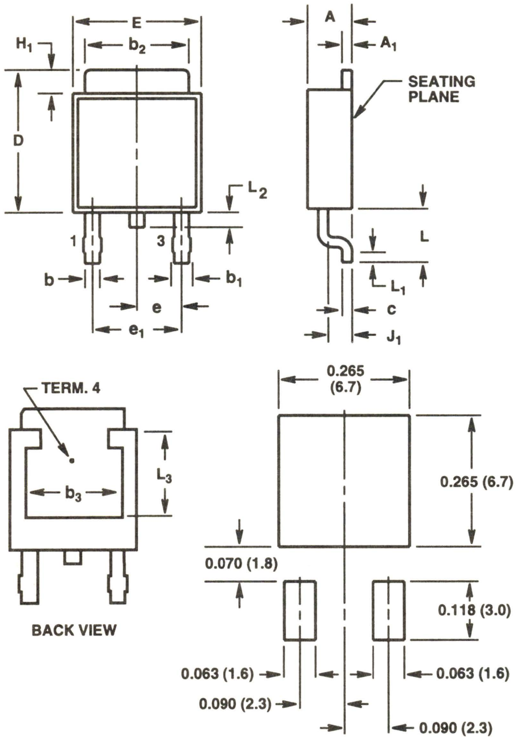
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b_1	0.033	0.040	0.84	1.01	3
b_2	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e_1	0.180 BSC		4.57 BSC		5
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L_1	0.075	0.090	1.91	2.28	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 10-95.

TO-252AA

SURFACE MOUNT JEDEC TO-252AA PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

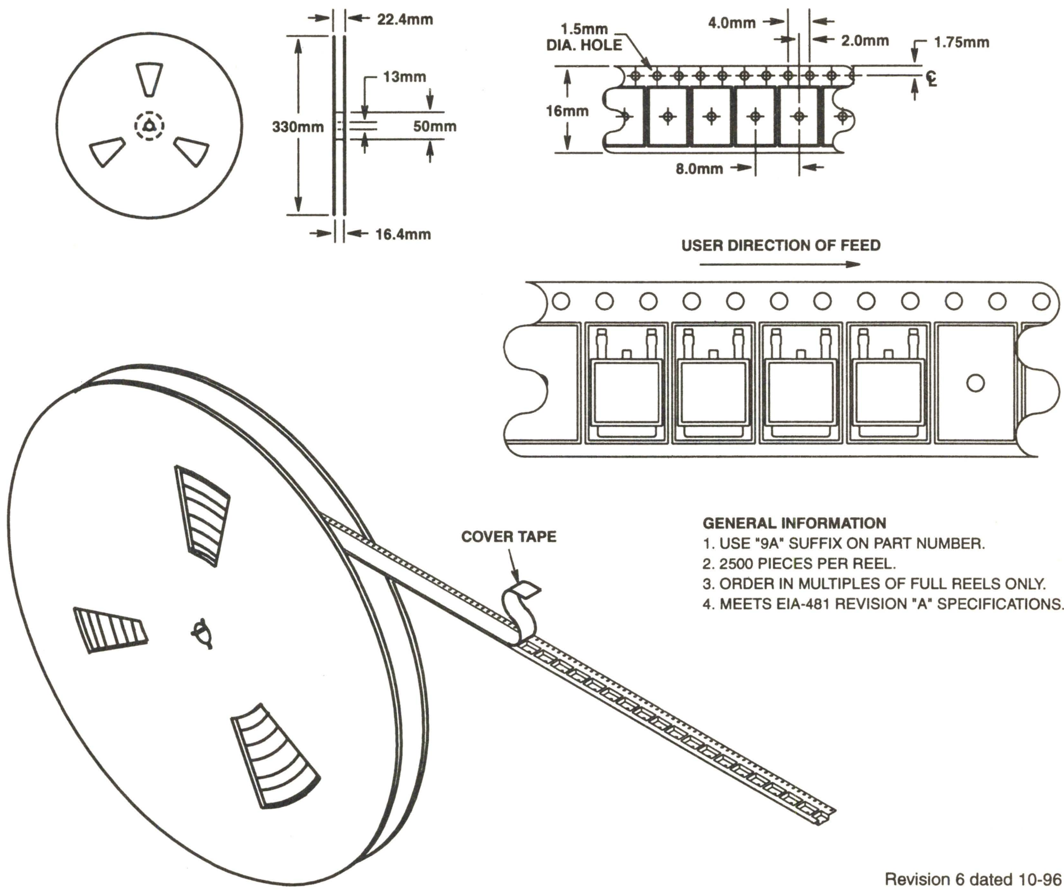
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b_1	0.033	0.040	0.84	1.01	4
b_2	0.205	0.215	5.21	5.46	4, 5
b_3	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e_1	0.180 BSC		4.57 BSC		7
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L_1	0.020	-	0.51	-	4, 6
L_2	0.025	0.040	0.64	1.01	3
L_3	0.170	-	4.32	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L_3 and b_3 dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 6 dated 10-96.

TO-252AA

16mm TAPE AND REEL



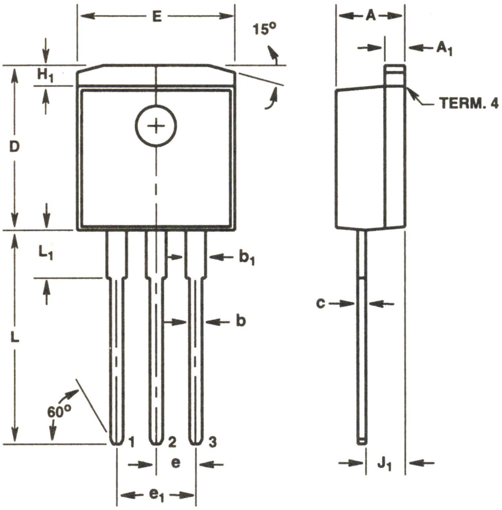
GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 6 dated 10-96

TO-262AA

3 LEAD JEDEC TO-262AA PLASTIC PACKAGE



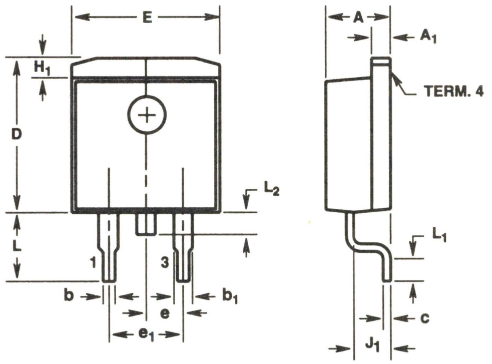
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	2

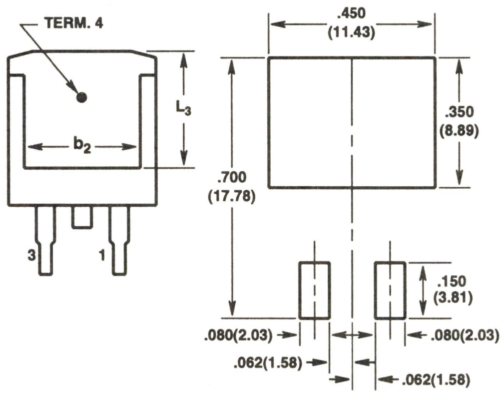
NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 4 dated 10-95.

TO-263AB

SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE





MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

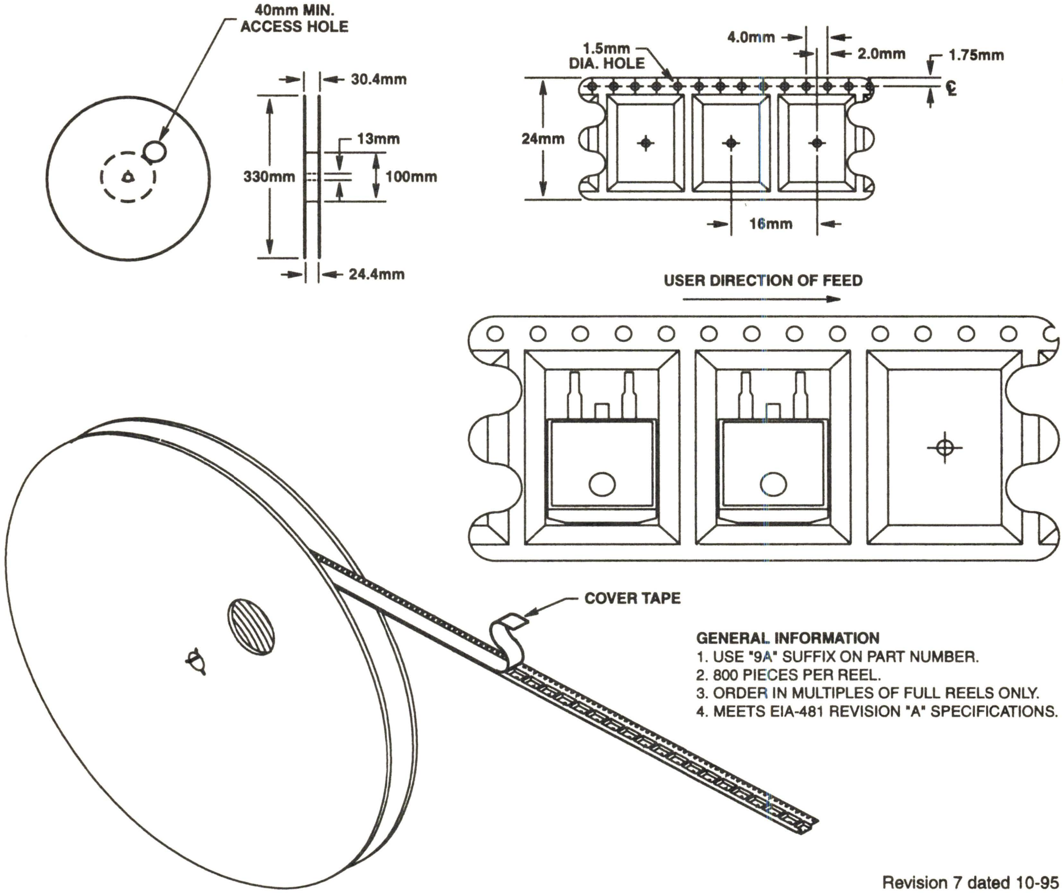
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4, 5
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	3
L_3	0.315	-	8.01	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 7 dated 10-95.

TO-263AB

24mm TAPE AND REEL



GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 800 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 7 dated 10-95

IGBT UFS SERIES SUPPLEMENT 9

HARRIS' ON-LINE SERVICES

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Your Map to Harris AnswerFAX	9-4
Harris AnswerFAX Data Book Request Form - Document #199	9-5
AnswerFAX Technical Support	9-6

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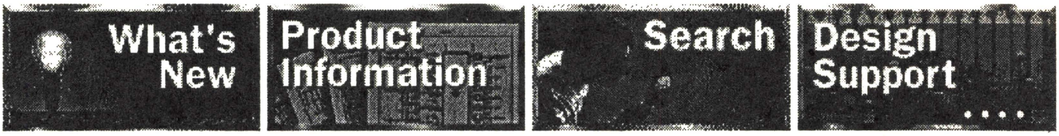
http://www.semi.harris.com/



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  - Data Sheets
- >2500 Data Sheets and Application Notes

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HARRIS SEMICONDUCTOR

ANSWER FAX[SM]

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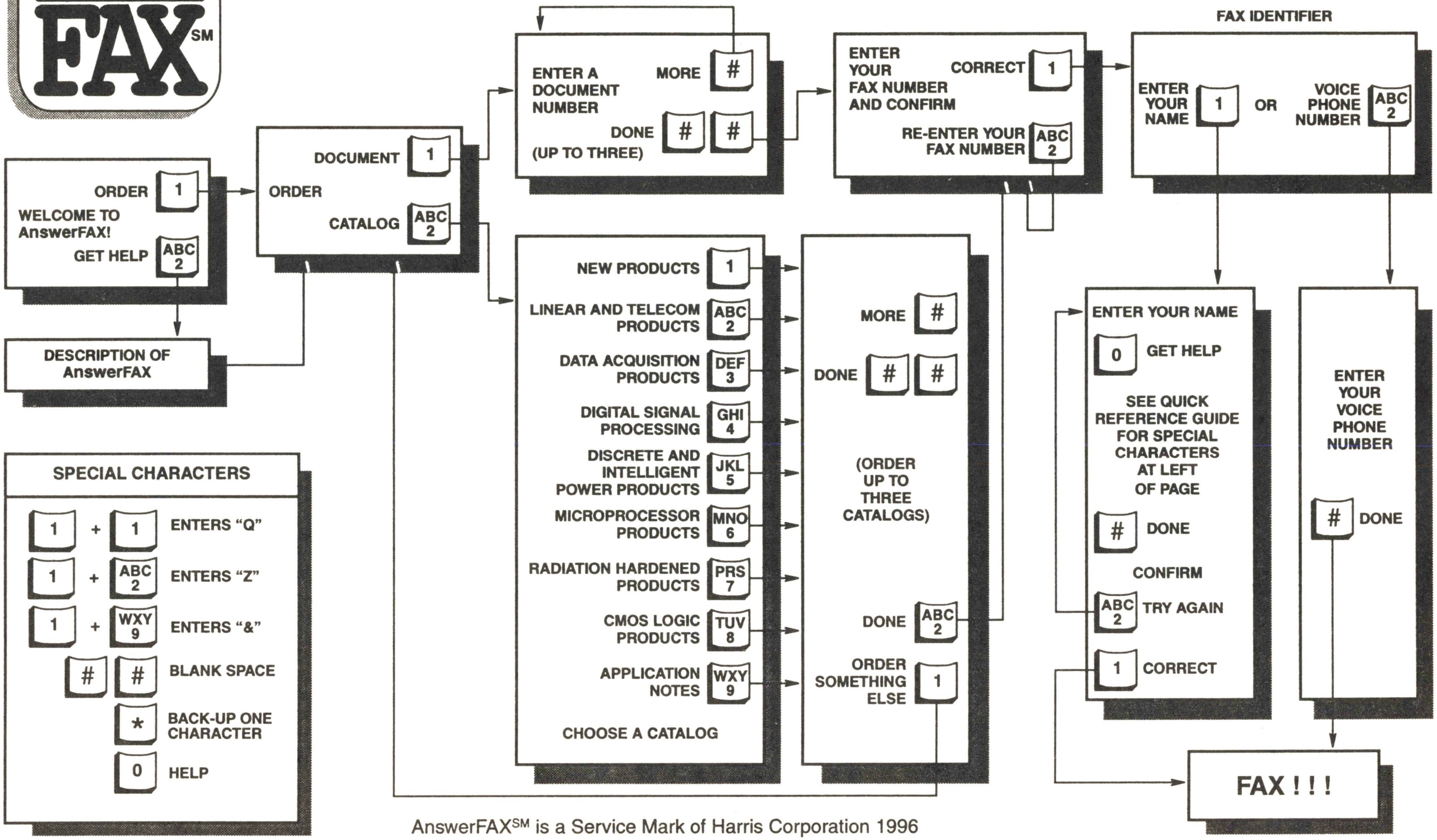
Please call 1-800-442-7747 and request extension number 7367.



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	DB316	**POWER MOSFET DATA BOOK SUPPLEMENT** (1996: 380pp) This data book contains the data sheets of recently introduced products and also updates some of the data sheets in the Power MOSFET Data Book DB223B. These data sheets contain the detailed specification for these products.
	DB235B	**RADIATION HARDENED** (1993: 2,232pp) The Harris radiation-hardened products include the CD4000, HCS/HCTS and ACS/ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog switches, gate arrays, standard cells and custom devices.
	DB260.2	**CDP6805 CMOS MICROCONTROLLERS & PERIPHERALS** (1995: 436pp) This data book represents the full line of Harris Semiconductor CDP6805 products for commercial applications and supersedes previously published CDP6805 data books under the Harris, GE, RCA or Intersil names.
	DB301B	**DATA ACQUISITION** (1994: 1,104pp) Product specifications on A/D converters (display, integrating, successive approximation, flash); D/A converters, switches, multiplexers, and other products.
	DB302B	**DIGITAL SIGNAL PROCESSING** (1994: 528pp) Product specifications on one-dimensional and two-dimensional filters, signal synthesizers, multipliers, special function devices (such as address sequencers, binary correlators, histogrammer).
	DB303	**MICROPROCESSOR PRODUCTS** (1992: 1,156pp) For commercial and military applications. Product specifications on CMOS microprocessors, peripherals, data communications, and memory ICs.
	DB304.1	**INTELLIGENT POWER ICs** (1994: 946pp) This data book includes a complete set of data sheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris quality and high reliability program.
	DB309.1	**MCT/IGBT/DIODES** (1995: 706pp) This MCT/IGBT/Diodes Data book represents the full line of these products made by Harris Semiconductor Discrete Power Products for commercial applications.
	DB319	**HARRIS IGBT UFS SERIES SUPPLEMENT** (1997: 164pp) The UFS series IGBT (Insulated Gate Bipolar Transistor) Data Book Supplement represents a new generation of IGBT products from Harris Semiconductor Discrete Power Products for commercial applications. This data book supplement describes Harris Semiconductor's line of UFS (Ultra Fast Switching) IGBTs.
	DB314	**SIGNAL PROCESSING NEW RELEASES** (1995: 690pp) This data book represents the newest products made by Harris Semiconductor Data Acquisition Products, Linear Products, Telecom Products and Digital Signal Processing Products for commercial applications.
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	DB318	**LPT/FCT CMOS LOGIC EXPANSION** (1997: 620pp) This data book fully describes Harris Semiconductor's LPT and FCT CMOS Logic ICs. It includes a complete set of data sheets for product specifications, application notes and techbriefs with design details for specific applications of Harris products, and a description of the Harris Quality and Reliability program.
	DB450.4	**TRANSIENT VOLTAGE SUPPRESSION DEVICES** (1995: 400pp) Product specifications of Harris varistors and surgectors. Also, general informational chapters such as: "Voltage Transients - An Overview," "Transient Suppression - Devices and Principles," "Suppression - Automotive Transients."
	DB500.3	**LINEAR ICs** (1996/97: 1446pp) Harris offers an extensive line of Linear components including: High Speed and General Purpose Op Amps, Comparators, Sample/Hold Amps, Video Crosspoint Switches, Special Analog Circuits and Transistor Arrays.
	Analog Military	**ANALOG MILITARY** (1989: 1,264pp) This data book describes Harris' military line of Linear, Data Acquisition, and Telecommunications circuits.
	DB312	**ANALOG MILITARY DATA BOOK SUPPLEMENT** (1994: 432pp) The 1994 Military Data Book Supplement, combined with the 1989 Analog Military Product Data Book, contain detailed technical information on the extensive line of Harris Semiconductor Linear and Data Acquisition products for Military (MIL-STD-883, DESC SMD and JAN) applications and supersedes all previously published Linear and Data Acquisition Military data books. For applications requiring Radiation Hardened products, please refer to the 1993 Harris Radiation Hardened Product Data Book (document #DB235B)
	PSG201.23	**PRODUCT SELECTION GUIDE** (1996: 834pp) Key product information on all Harris Semiconductor devices. Sectioned (Linear, Data Acquisition, Digital Signal Processing, Telecom, Intelligent Power, Discrete Power, Digital Microprocessors and Hi-Rel/Military and Rad Hard) for easy use and includes cross references and alphanumeric part number index.
	SG103	**CMOS LOGIC SELECTION GUIDE** (1994: 288pp) This product selection guide contains technical information on Harris Semiconductor High Speed 54/74 CMOS Logic Integrated Circuits for commercial, industrial and military applications. It covers Harris' High Speed CMOS Logic HC/HCT Series, AC/ACT Series, BiCMOS Interface Logic FCT Series and CMOS Logic CD4000B Series.
	BR-057.3	**AnswerFAX CATALOG** (Fall 1996: 112pp) A Complete AnswerFAX Catalog listing.

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APPLICATION NOTE LISTING

AnswerFAX DOCUMENT NUMBER	APPLICATION NOTE	TITLE
98602	**(General IGBTs)** AN8602	The IGBTs - A New High Conductance MOS-Gated Device (3 pages) AN8602.1
98603	**(General IGBTs)** AN8603	Improved IGBTs with Fast Switching Speed And High-Current Capability (4 pages) AN8603.2
99318	**(General IGBTs)** AN9318	Insulated-Gate Transistors Simplify AC-Motor Speed Control (12 pages) AN9318
99319	**(General IGBTs)** AN9319	Parallel Operation Of Insulated Gate Transistors (6 pages) AN9319
99408	**(General IGBTs, MCTs), HIP2030** AN9408	The HIP2030 MCT/IGBT Gate Driver Provides Isolated Control Signals To Switch Power Devices (7 pages) AN9408.2
97332	**(General MOSFETs)** AN7332	The Application Of Conductivity-Modulated Field-Effect Transistors (5 pages) AN7332.1
99320	**(General MOSFETs & IGBTs)** AN9320	Parallel Operation Of Semiconductor Switches (4 pages) AN9320
99010	**HIP2500** AN9010	HIP2500 High Voltage (500VDC) Half-Bridge Driver IC (8 pages)
99335	**HIP5500** AN9335	HIP5500 High Voltage (500VDC) Power Supply Driver IC (13 pages)
99301	**HV400, ICL7667** AN9301	High Current Logic Level MOSFET Driver (3 pages)
98829	**SP600, SP601** AN8829	SP600 and SP601 an HVIC MOSFET/IGT Driver for Half-Bridge Topologies (6 pages)
99105	**SP601** AN9105	HVIC/IGBT Half-Bridge Converter Evaluation Circuit (1 page)
82334	**(General Power)** TB334	Guidelines for Soldering Surface Mount Components to PC Boards (2 pages) TB334

For more information, see the AnswerFAX map on page 9-4 and choose catalog item #5, “Discrete and Intelligent Power Products”.

IGBT UFS SERIES SUPPLEMENT 10

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